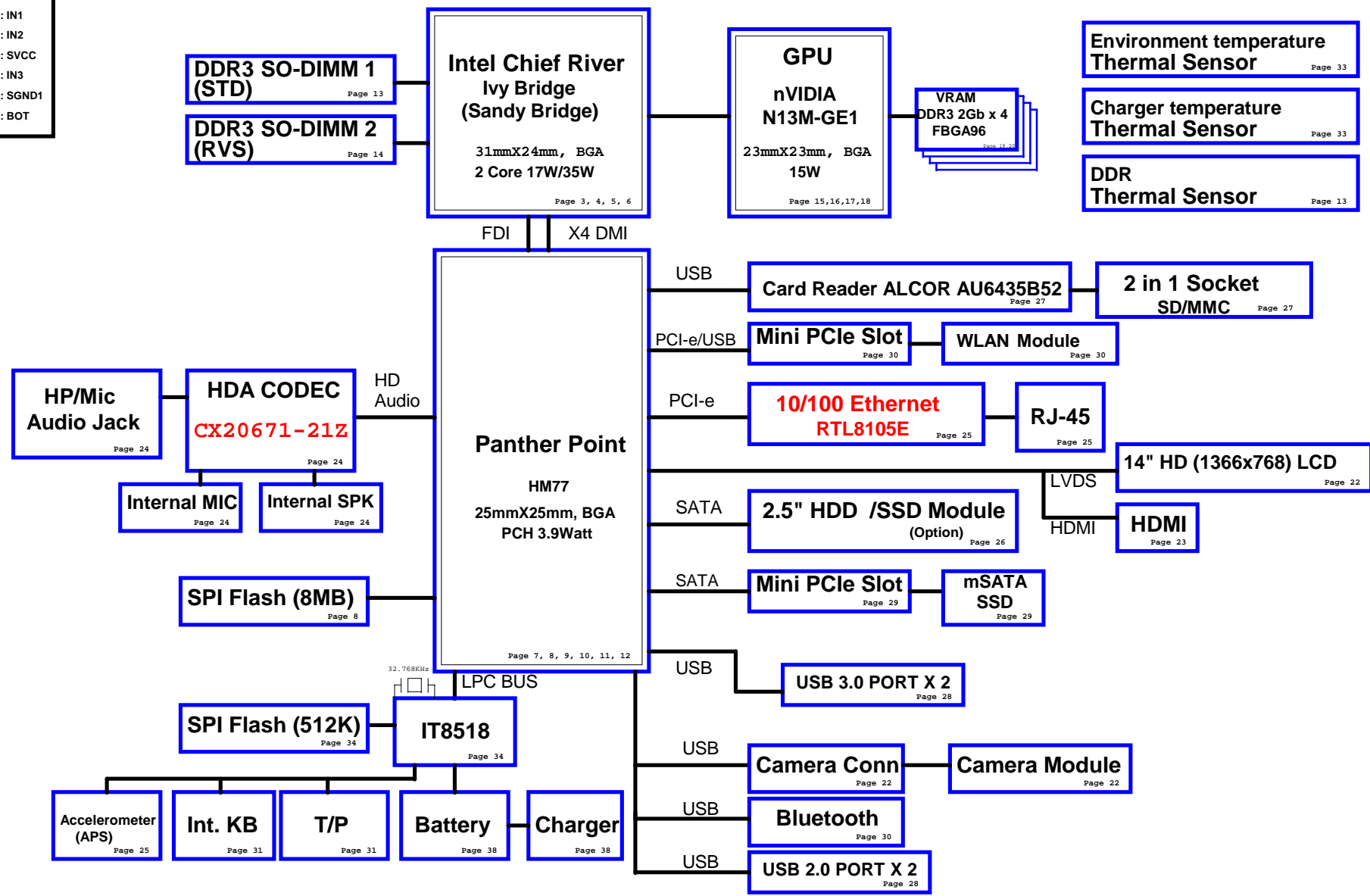


- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : IN3
- LAYER 7 : SGND1
- LAYER 8 : BOT

LZ8 14" Block Diagram -- Intel Chief River ULV



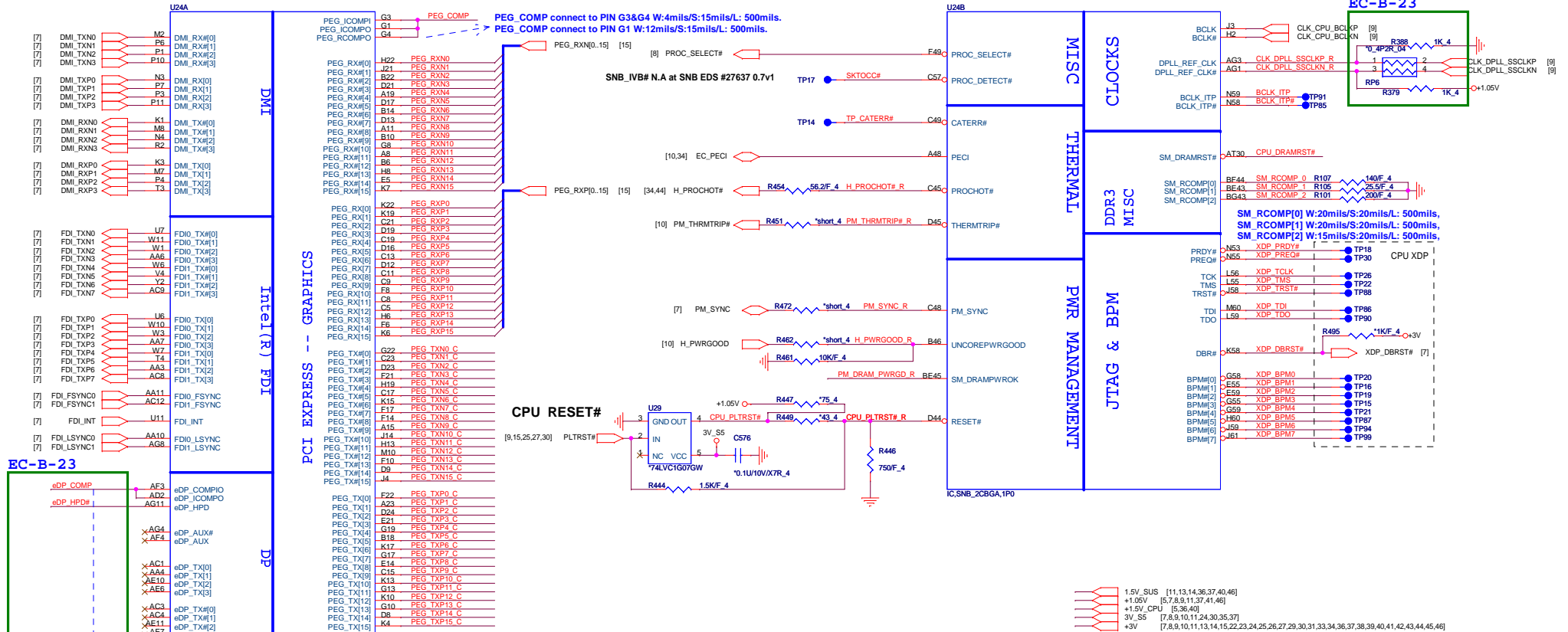
POWER	
DC/DC	3V_PCU, 5V_PCU, +15V Page 39
REGULATOR (DDR3)	1.5V_SUS, 0.75V_DDR_VTT Page 40
REGULATOR	1.05V Page 41
REGULATOR	VCCSA Page 42
CPU Core	Page 44
Charger	Page 38
RUN POWER SW/Discharge	5V_SUS, 3V_S5, 5V_S5 +3V, +5V Page 37
REGULATOR	1.8V Page 43
dGPU Core	Page 45,46

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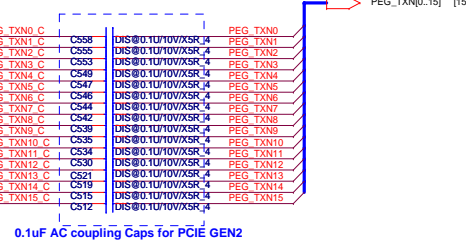
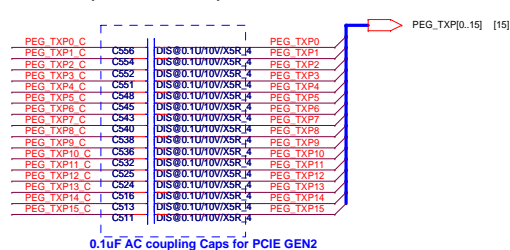
PAGE	DESCRIPTION
01	BLOCK DIAGRAM
02	FRONT PAGE
03-06	IVY/Sandy Bridge
07-12	Panther/Cougar Point-PCH
13-14	DDR3 SO-DIMM
15-18	N13M
19-20	N13M VRAM
21	PS8622 LVDS converter
22	LCD/CAMERA
23	HDMI CONN
24	Audio Codec CX20672
25	LAN[RTL8105E]
26	SATA
27	Card Reader-AU6435B52-GDL
28	USB2.0 X2/USB3.0 X2
29	MINI Card (SSD)
30	WLAN/BT
31	KB/TP/LID
32	USB2.0--Audio Jack conn
33	FAN/Thermal
34	KBC IT8518
35	SW/LED
36	Screw Hole/EMI/ESD
37	Discharge
38	CHARGER (bq24725A)
39	3V/5V (TPS51123ARGER)
40	DDR3/0.75V (TPS51216)
41	1.05V_PCH(RT8240B)
42	VCCSA (RT8241A)
43	1.8V(TPS54318)
44	CPU(ISL95831)IMVP2+1
45	DGPU CORE(TPS51728)
46	GPU
47	
48	
49	
50	
51	

Power States

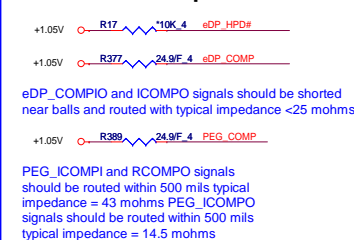
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	22,36,38,39,40,41,42,44,45	MAIN POWER		S0~S5
+3V_RTC	+3.0V~+3.3V	7,8,11,34	RTC		S0~S5
3VPCU	+3.3V	7,8,22,23,25,30,31,34,35,36,37,38,39,43,45	IT8518/19 POWER	3V5V_EN	S0~S5
5VPCU	+5V	22,36,37,39,40,41,42,43,44,45,46	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
15V	+15V	22,37,39,40,46	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	25,37	LAN POWER	LAN_ON	
5V_S5	+5V	11,24,28,32,37	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	3,7,8,9,10,11,30,35,37,45	Sys Management,PCH Resume Well, USB,WLAN,WiMAX POWER	S5_ON	S0~S3
1.5V_SUS	+1.5V	3,11,13,14,36,37,40,46	DDR3 SODIMM POWER	SUSON	S0~S3
+0.75V_DDR_VTT	+0.75V	13,14,37,40	DDR3 SODIMM REFERENCE POWER	MAINON	S0
+5V	+5V	7,8,11,22,23,24,26,31,33,36,37,38	SLP_S3# CTRLD POWER	MAINON	S0
+3V	+3.3V	3,7,8,9,10,11,13,14,15,21,22,23,24,25,26,27,29,30,31,33,34,35,36,37,38,39,40,41,42,43,44,45,46	SLP_S3# CTRLD POWER	MAINON	S0
VCC_GFX		5,36,44	VGA CORE POWER	MAINON	S0
VCCSA	+0.8V~+0.9V	5,37,42	Sandy Bridge Power	MAINON	S0
+1.8V	+1.8V	5,8,11,37,43	LVDS,NVM POWER	MAINON	S0
+1.05V	+1.05V	3,5,7,8,9,11,21,36,37,41,46	Sandy Bridge VTT POWER/PCH CORE POWER	MAINON	S0
VCC_CORE		5,6,36,44	CPU CORE POWER	VRON	S0
+LCDVCC	+3.3V	22	LCD Power	ENVDD	S0
+3V_HDD	+3V	26	ODD Power	ODD_5V_ON	S0
+5V_HDD	+5V	26	HDD Power	MAINON#	S0
BAT-V	+10V~+17V	38	MAIN BATTERY	CHG_PBATT	S0~S5
+1.5V_CPU	+1.5V	3,5,36	DDR3 1.5V Rails	PS_S3CNTRL	S0



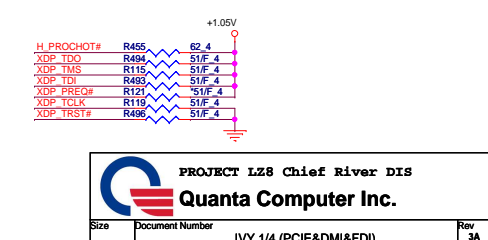
PEG x16 (UMA Non-stuff)



DP & PEG Compensation

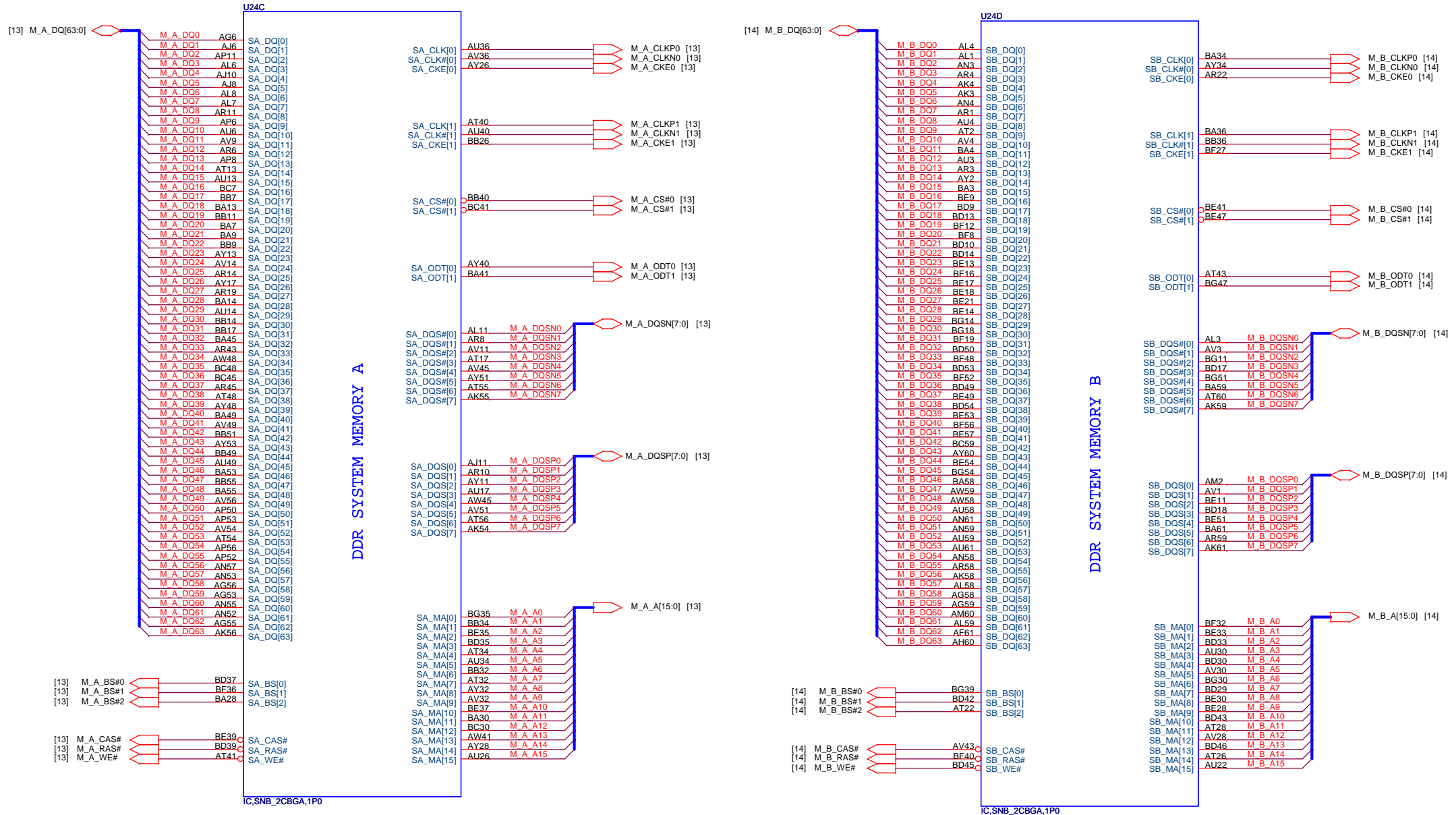


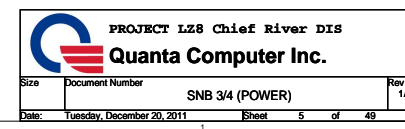
Processor pull-up (CPU)



Ivy/Sandy Bridge Processor (DDR3)

04

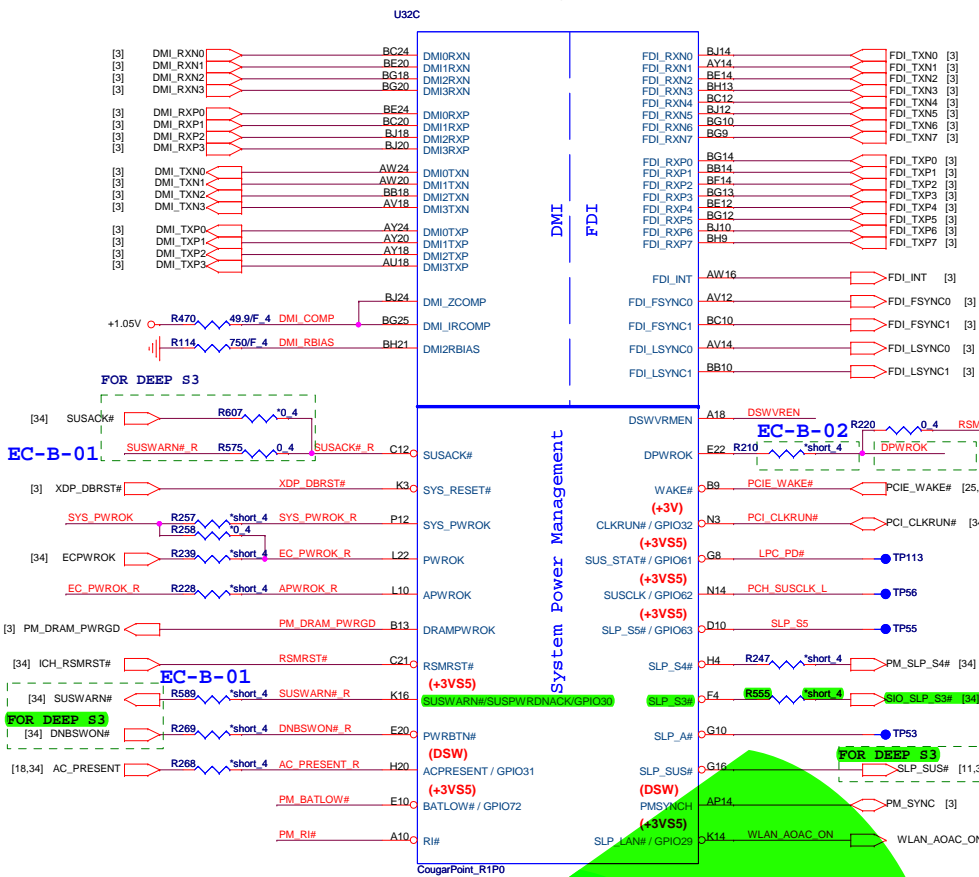




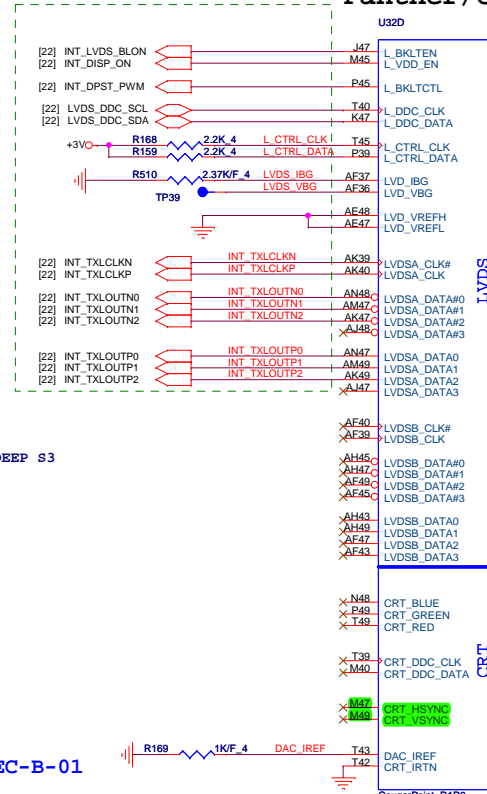
06



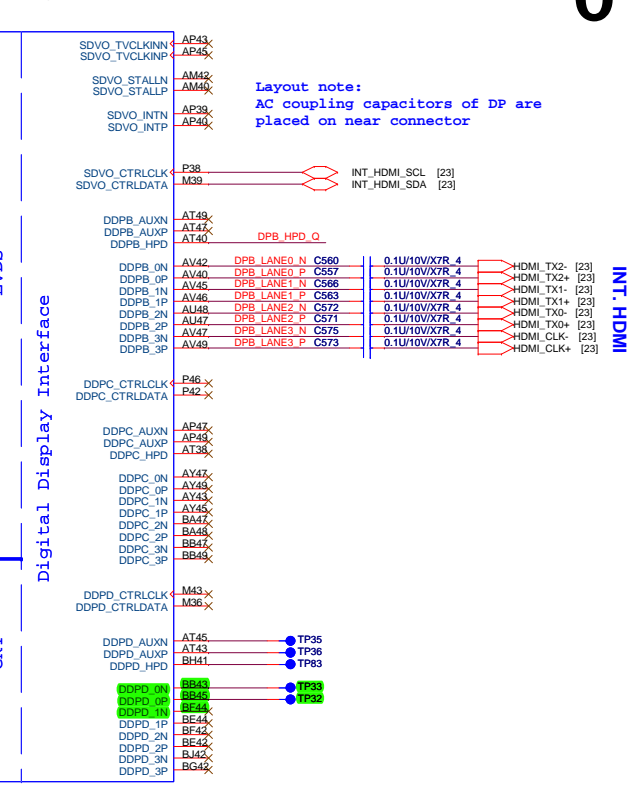
Panther/Cougar Point (DMI, FDI, PM)



EC-B-23



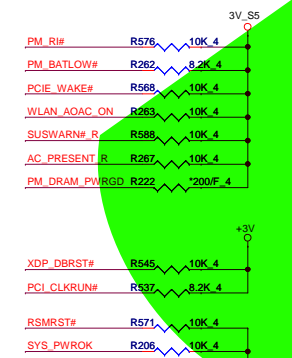
Panther/Cougar Point (LVDS, DDI)



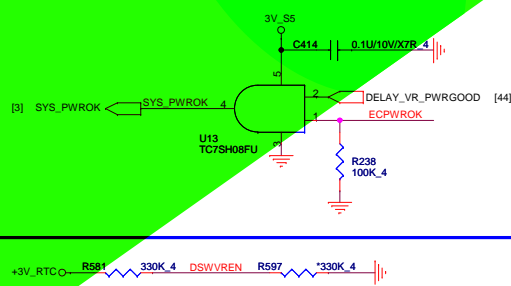
Layout note:
AC coupling capacitors of DP are
placed on near connector

INT. HDMI

PCH Pull-high/low(CLG)

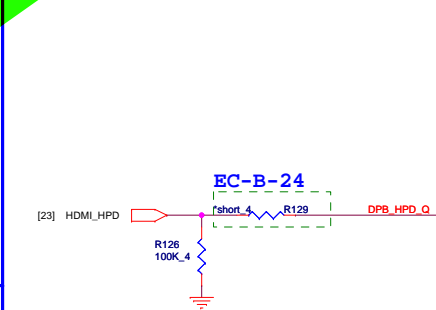


System PWR_OK(CLG)



On Die DSW VR Enable
High = Enable (Default) Low = Disable

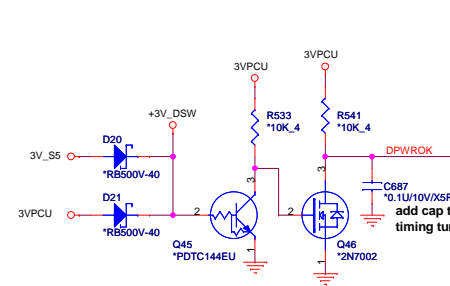
INT HDMI DETECT



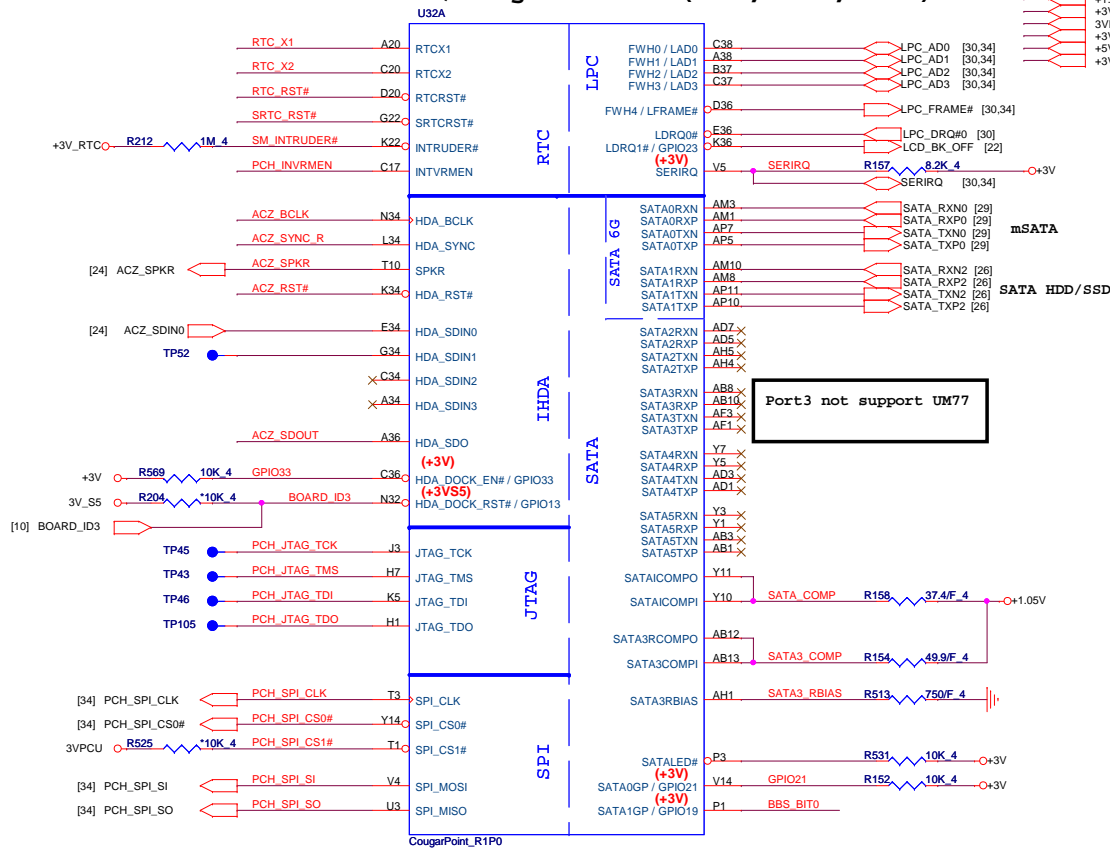
LVDS for HM76

EC-B-23

DPWROK FOR DSW (DEEP S3)



Panther/Cougar Point (HDA,JTAG,SATA)



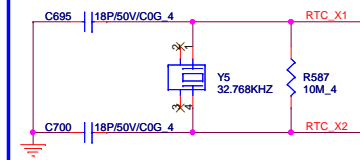
if default boot destination is SPI,
no external pull-up/-down resistors on the board are
necessary

PCH Strap Table

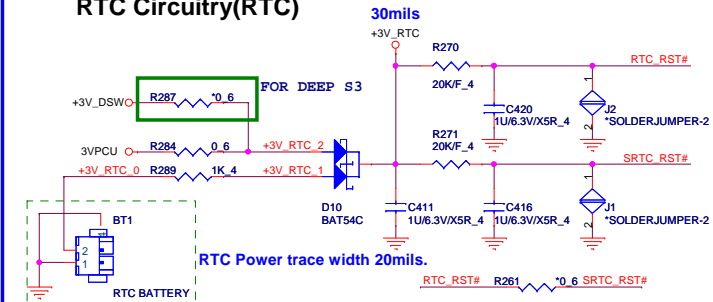
Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR <div>Different from Calpella</div>	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
HDA_SDO <div>Flash Descriptor Security Only for Interposer</div>		PWROK	0 = effective(Default: weak pull down) 1 = Override										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>0</td><td>SPI</td></tr><tr><td>0</td><td>1</td><td>LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	1	0	SPI	0	1	LPC	<div>[Need external pull-down for LPC BIOS]</div>
GNT1#	GNT0#	Boot Location											
1	0	SPI											
0	1	LPC											
GPIO19 <div>Different from Calpella</div>	Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
DF_TVS	DMI Termination voltage	PWROK	weak pull-down 20kohm										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite		Low = Disable (Default) High = Enable										
GPIO28 <div>Different from Calpella</div>	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
DSWVREN	0: disable 1: enable												

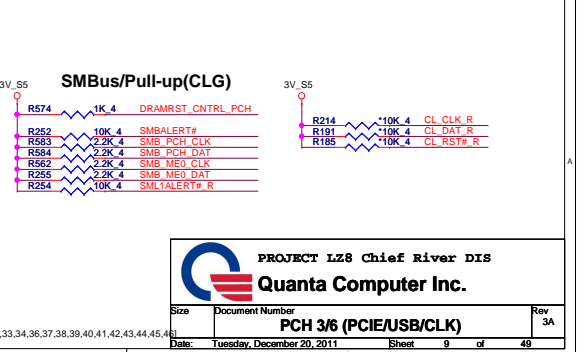
RTC Clock 32.768KHz

08

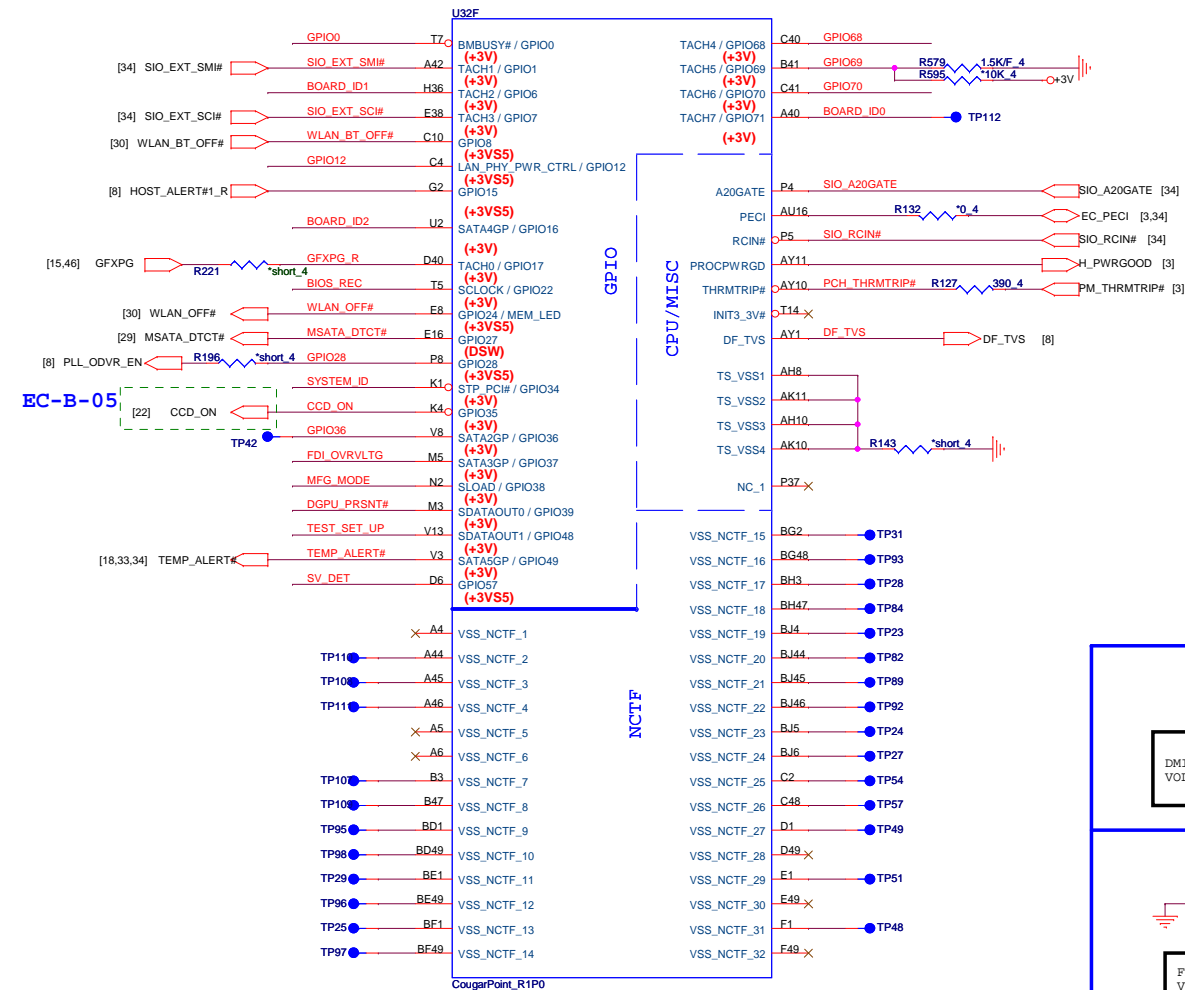


RTC Circuitry(RTC)





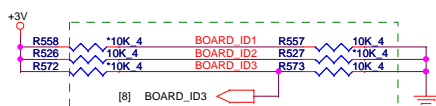
Panther/Cougar Point (GPIO,VSS_NCTF,RSVD)



3V_S5 +3V [3,7,8,9,11,24,30,35,37] [3,7,8,9,11,13,14,15,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]

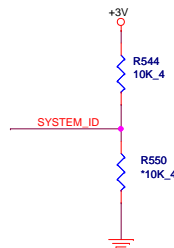
BOARD ID SETTING

Board ID For Function	ID1 GPIO6	ID2 GPIO16	ID3 GPIO13
SDV	0	0	0
SIV	0	0	1
SIT	0	1	0
SVT			
SOVP			



EC-B-04
EC-C-02

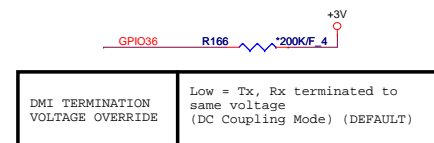
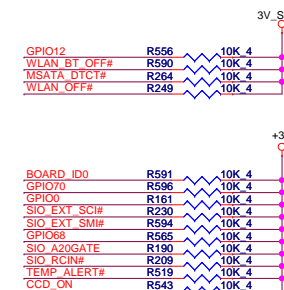
	SYSTEM_ID
L27	0
L28	1



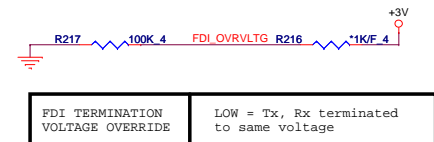
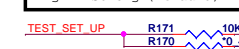
3V_S5 +3V [3,7,8,9,11,24,30,35,37] [3,7,8,9,11,13,14,15,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]

10

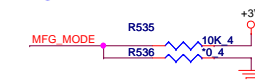
GPIO Pull-up/Pull-down(CLG)



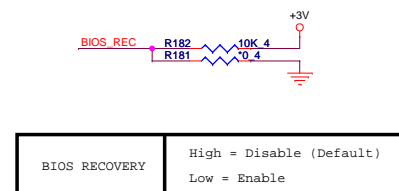
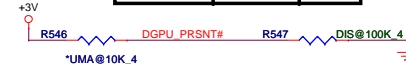
SV_SET_UP
High = Strong (Default)



MFG-TEST



	Optimus	UMA
Stuff	R547	R546
No Stuff	R546	R547

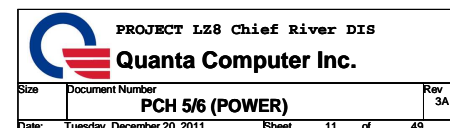


PROJECT L28 Chief River DIS
Quanta Computer Inc.

Size: Document Number: PCH 4/6 (GPIO/MISC) Rev: 3A

Date: Tuesday, December 20, 2011 Sheet: 10 of 49

Panther/COUGAR POINT (POWER)



Panther/Cougar Point-M (GND)

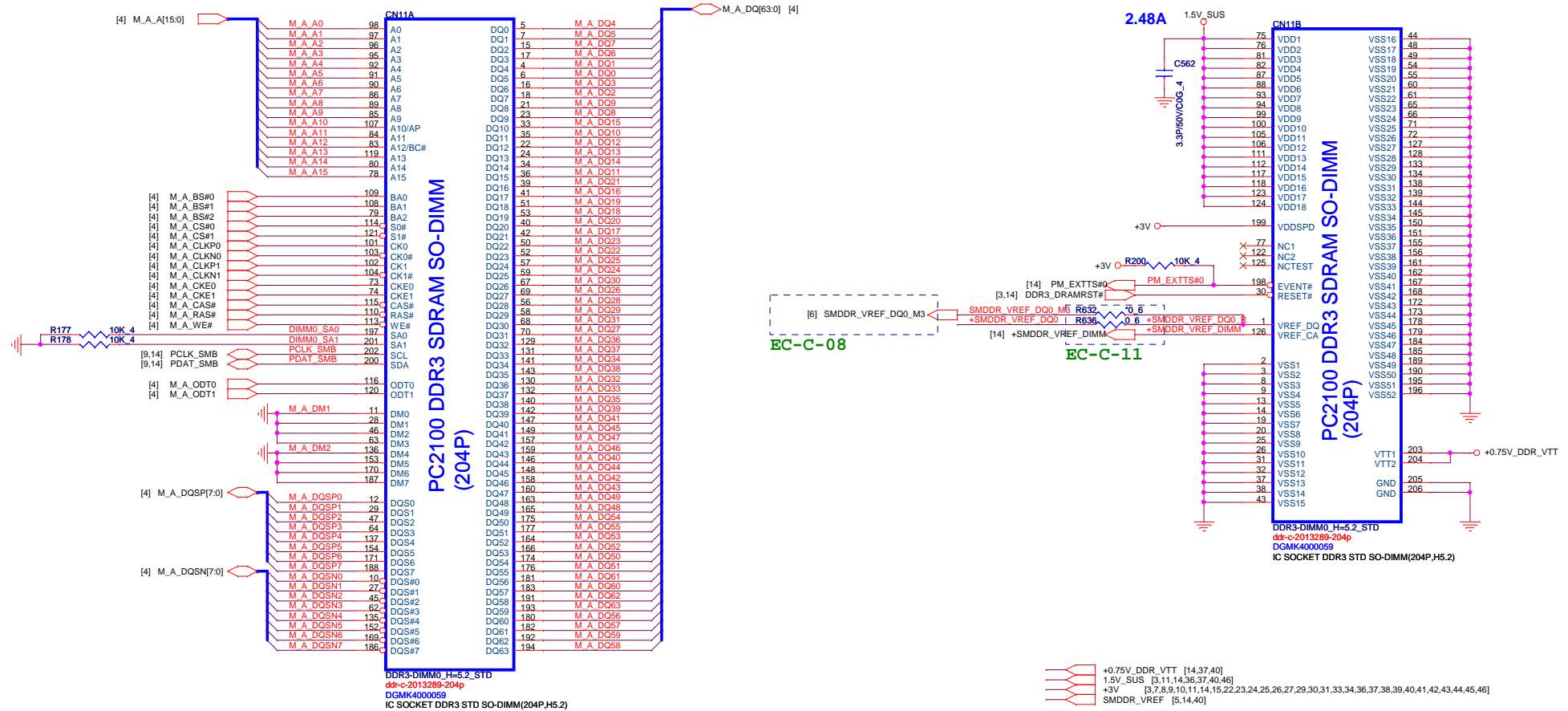
U321		
AY4	VSS[159]	VSS[259] H46
AY42	VSS[160]	VSS[260] K18
AY46	VSS[161]	VSS[261] K26
AY8	VSS[162]	VSS[262] K39
B11	VSS[163]	VSS[263] K46
B15	VSS[164]	VSS[264] K7
B19	VSS[165]	VSS[265] L18
B23	VSS[166]	VSS[266] L2
B27	VSS[167]	VSS[267] L20
B31	VSS[168]	VSS[268] L26
B35	VSS[169]	VSS[269] L28
B39	VSS[170]	VSS[270] L36
B7	VSS[171]	VSS[271] L48
F45	VSS[172]	VSS[272] M12
BB12	VSS[173]	VSS[273] P16
BB16	VSS[174]	VSS[274] M18
BB20	VSS[175]	VSS[275] M22
BB22	VSS[176]	VSS[276] M24
BB24	VSS[177]	VSS[277] M30
BB28	VSS[178]	VSS[278] M32
BB30	VSS[179]	VSS[279] M34
BB38	VSS[180]	VSS[280] M38
BB4	VSS[181]	VSS[281] M4
BB46	VSS[182]	VSS[282] M42
BC14	VSS[183]	VSS[283] M46
BC18	VSS[184]	VSS[284] M8
BC2	VSS[185]	VSS[285] N18
BC22	VSS[186]	VSS[286] P30
BC26	VSS[187]	VSS[287] N47
BC32	VSS[188]	VSS[288] P11
BC34	VSS[189]	VSS[289] P18
BC36	VSS[190]	VSS[290] T33
BC40	VSS[191]	VSS[291] P40
BC42	VSS[192]	VSS[292] P43
BC48	VSS[193]	VSS[293] P47
BD46	VSS[194]	VSS[294] P7
BD5	VSS[195]	VSS[295] R2
BE22	VSS[196]	VSS[296] R48
BE26	VSS[197]	VSS[297] T12
BE40	VSS[198]	VSS[298] T31
BE10	VSS[199]	VSS[299] T37
BE12	VSS[200]	VSS[300] T4
BE16	VSS[201]	VSS[301] W34
BF20	VSS[202]	VSS[302] T46
BF22	VSS[203]	VSS[303] T47
BF24	VSS[204]	VSS[304] T8
BF26	VSS[205]	VSS[305] V11
BF28	VSS[206]	VSS[306] V17
BD3	VSS[207]	VSS[307] V26
BF40	VSS[208]	VSS[308] V27
BF38	VSS[209]	VSS[309] V29
BF40	VSS[210]	VSS[310] V31
BF8	VSS[211]	VSS[311] V36
BG17	VSS[212]	VSS[312] V39
BG21	VSS[213]	VSS[313] V43
BG33	VSS[214]	VSS[314] V7
BG44	VSS[215]	VSS[315] W17
BG8	VSS[216]	VSS[316] W19
BH11	VSS[217]	VSS[317] W2
BH15	VSS[218]	VSS[318] W27
BH17	VSS[219]	VSS[319] W48
BH19	VSS[220]	VSS[320] Y12
H10	VSS[221]	VSS[321] Y38
BH27	VSS[222]	VSS[322] Y4
BH31	VSS[223]	VSS[323] Y42
BH33	VSS[224]	VSS[324] Y46
BH35	VSS[225]	VSS[325] Y8
BH39	VSS[226]	VSS[326] BG29
BH43	VSS[227]	VSS[327] N24
BH7	VSS[228]	VSS[328] AJ3
D3	VSS[229]	VSS[329] AD47
D12	VSS[230]	VSS[330] AH11
D16	VSS[231]	VSS[331] AH3
D18	VSS[232]	VSS[332] AH36
D22	VSS[233]	VSS[333] B43
D24	VSS[234]	VSS[334] BE10
D26	VSS[235]	VSS[335] AH40
D30	VSS[236]	VSS[336] AH42
D32	VSS[237]	VSS[337] AH46
D34	VSS[238]	VSS[338] AH7
D38	VSS[239]	VSS[339] AJ19
D42	VSS[240]	VSS[340] T36
D8	VSS[241]	VSS[341] AJ21
E18	VSS[242]	VSS[342] AJ24
E26	VSS[243]	VSS[343] C22
G18	VSS[244]	VSS[344] AP13
G20	VSS[245]	VSS[345] M14
G26	VSS[246]	VSS[346] AP3
G28	VSS[247]	VSS[347] AP1
G36	VSS[248]	VSS[348] BE16
G48	VSS[249]	VSS[349] BC16
H12	VSS[250]	VSS[350] BG28
H18	VSS[251]	VSS[351] BJ28
H22	VSS[252]	VSS[352]
H24	VSS[253]	
H26	VSS[254]	
H30	VSS[255]	
H32	VSS[256]	
H34	VSS[257]	
F3	VSS[258]	

CougarPoint_R1P0

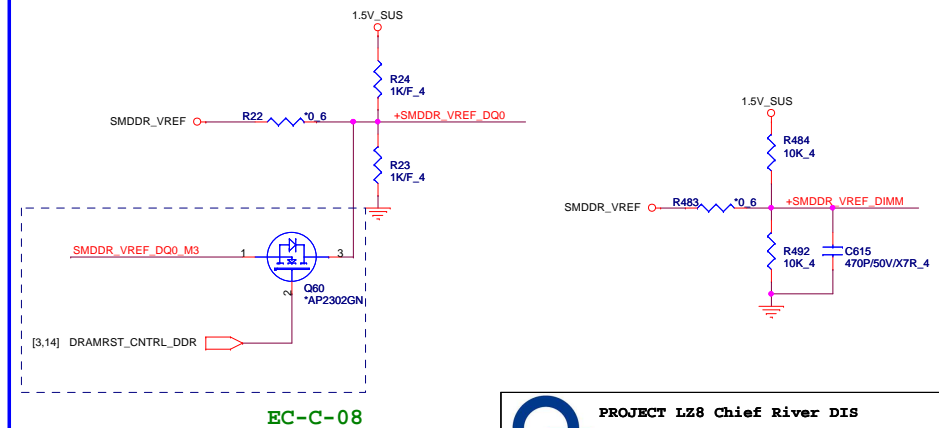
Panther/Cougar Point-M (GND)

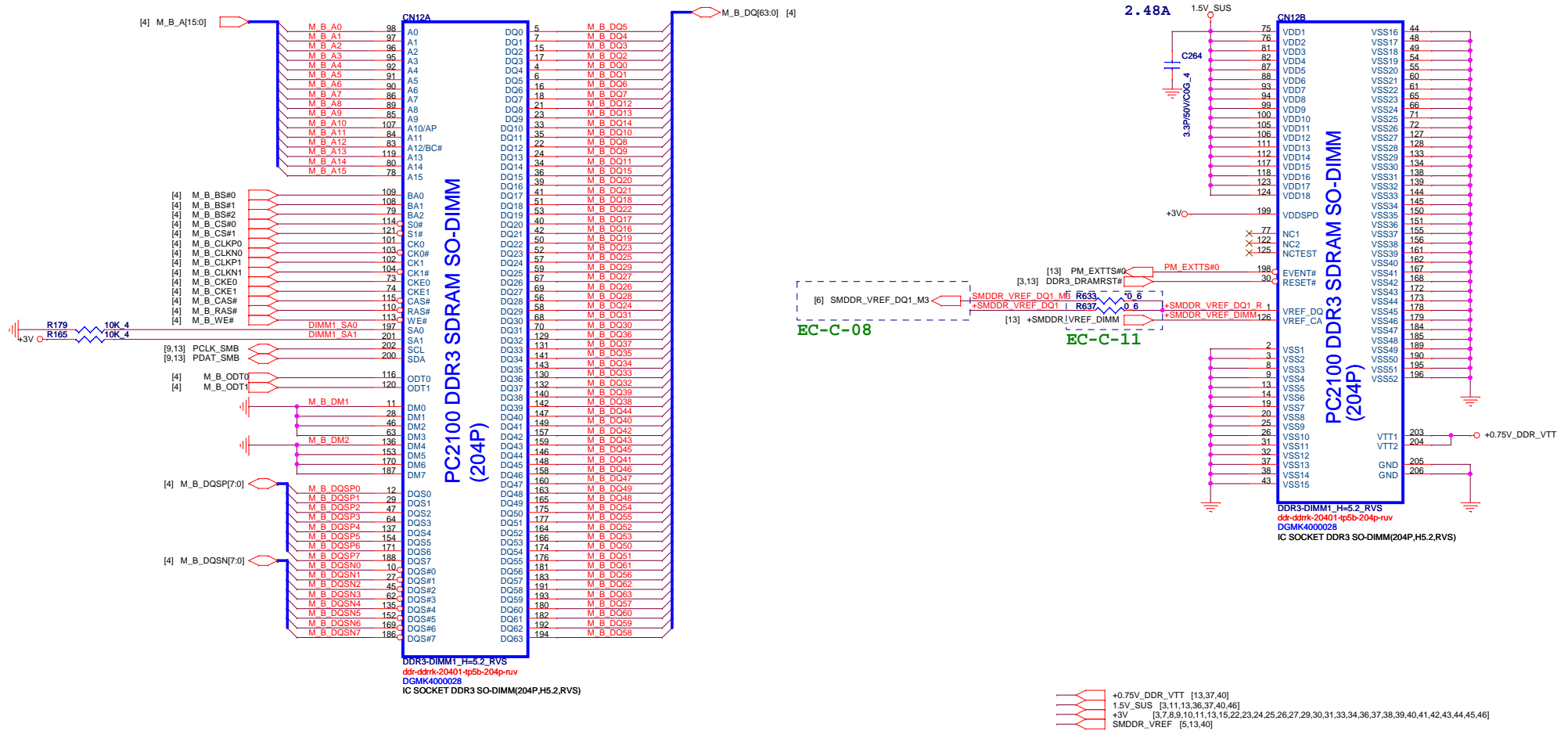
U32H		
H5	VSS[0]	
AA17	VSS[1]	VSS[80] AK38
AA2	VSS[2]	VSS[81] AK4
AA3	VSS[3]	VSS[82] AK42
AA33	VSS[4]	VSS[83] AK46
AA34	VSS[5]	VSS[84] AK8
AB11	VSS[6]	VSS[85] AL16
AB14	VSS[7]	VSS[86] AL17
AB39	VSS[8]	VSS[87] AL19
AB4	VSS[9]	VSS[88] AL2
AB43	VSS[10]	VSS[89] AL21
AB5	VSS[11]	VSS[90] AL23
AB7	VSS[12]	VSS[91] AL25
AC19	VSS[13]	VSS[92] AL27
AC2	VSS[14]	VSS[93] AL31
AC21	VSS[15]	VSS[94] AL33
AC24	VSS[16]	VSS[95] AL34
AC33	VSS[17]	VSS[96] AL48
AC34	VSS[18]	VSS[97] AM11
AC48	VSS[19]	VSS[98] AM14
AD10	VSS[20]	VSS[99] AM36
AD11	VSS[21]	VSS[100] AM39
AD12	VSS[22]	VSS[101] AM43
AD13	VSS[23]	VSS[102] AM45
AD19	VSS[24]	VSS[103] AM46
AD24	VSS[25]	VSS[104] AM7
AD26	VSS[26]	VSS[105] AN2
AD27	VSS[27]	VSS[106] AN29
AD33	VSS[28]	VSS[107] AN3
AD34	VSS[29]	VSS[108] AN31
AD36	VSS[30]	VSS[109] AP12
AD37	VSS[31]	VSS[110] AP19
AD38	VSS[32]	VSS[111] AP28
AD39	VSS[33]	VSS[112] AP30
AD4	VSS[34]	VSS[113] AP32
AD40	VSS[35]	VSS[114] AP38
AD42	VSS[36]	VSS[115] AP4
AD43	VSS[37]	VSS[116] AP42
AD45	VSS[38]	VSS[117] AP46
AD46	VSS[39]	VSS[118] AP8
AD8	VSS[40]	VSS[119] AR2
AE2	VSS[41]	VSS[120] AR48
AE3	VSS[42]	VSS[121] AT11
AF10	VSS[43]	VSS[122] AT13
AF12	VSS[44]	VSS[123] AT18
AD14	VSS[45]	VSS[124] AT22
AD16	VSS[46]	VSS[125] AT26
AF18	VSS[47]	VSS[126] AT28
AF19	VSS[48]	VSS[127] AT30
AF24	VSS[49]	VSS[128] AT32
AF26	VSS[50]	VSS[129] AT34
AF27	VSS[51]	VSS[130] AT39
AF28	VSS[52]	VSS[131] AT42
AF31	VSS[53]	VSS[132] AT46
AF38	VSS[54]	VSS[133] AT7
AF4	VSS[55]	VSS[134] AU24
AF42	VSS[56]	VSS[135] AU30
AF46	VSS[57]	VSS[136] AV16
AF5	VSS[58]	VSS[137] AV20
AF7	VSS[59]	VSS[138] AV24
AF8	VSS[60]	VSS[139] AV30
AG19	VSS[61]	VSS[140] AV38
AG2	VSS[62]	VSS[141] AV4
AG31	VSS[63]	VSS[142] AV43
AG48	VSS[64]	VSS[143] AV8
AH11	VSS[65]	VSS[144] AW14
AH3	VSS[66]	VSS[145] AW18
AH36	VSS[67]	VSS[146] AW2
B43	VSS[68]	VSS[147] AW22
BE10	VSS[69]	VSS[148] AW26
AH40	VSS[70]	VSS[149] AW28
AH42	VSS[71]	VSS[150] AW32
AH46	VSS[72]	VSS[151] AW34
AH7	VSS[73]	VSS[152] AW36
AJ19	VSS[74]	VSS[153] AW40
AJ21	VSS[75]	VSS[154] AW48
AJ24	VSS[76]	VSS[155] AV11
AJ33	VSS[77]	VSS[156] AV12
AJ34	VSS[78]	VSS[157] AY22
AK12	VSS[79]	VSS[158] AY28
AK3		

CougarPoint_R1P0

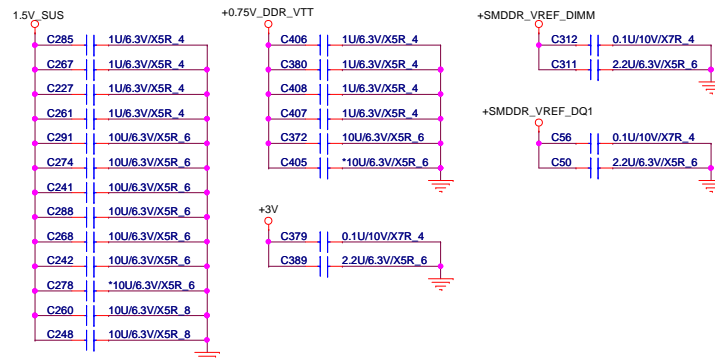


VREF DQ0 M1/M3 Solution

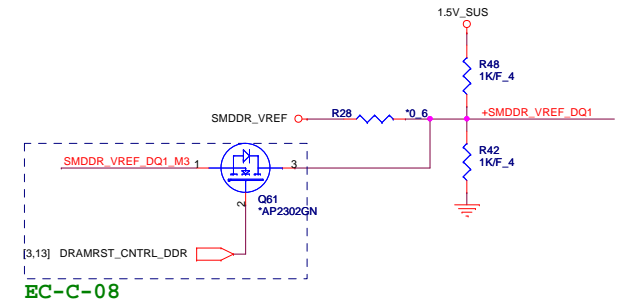


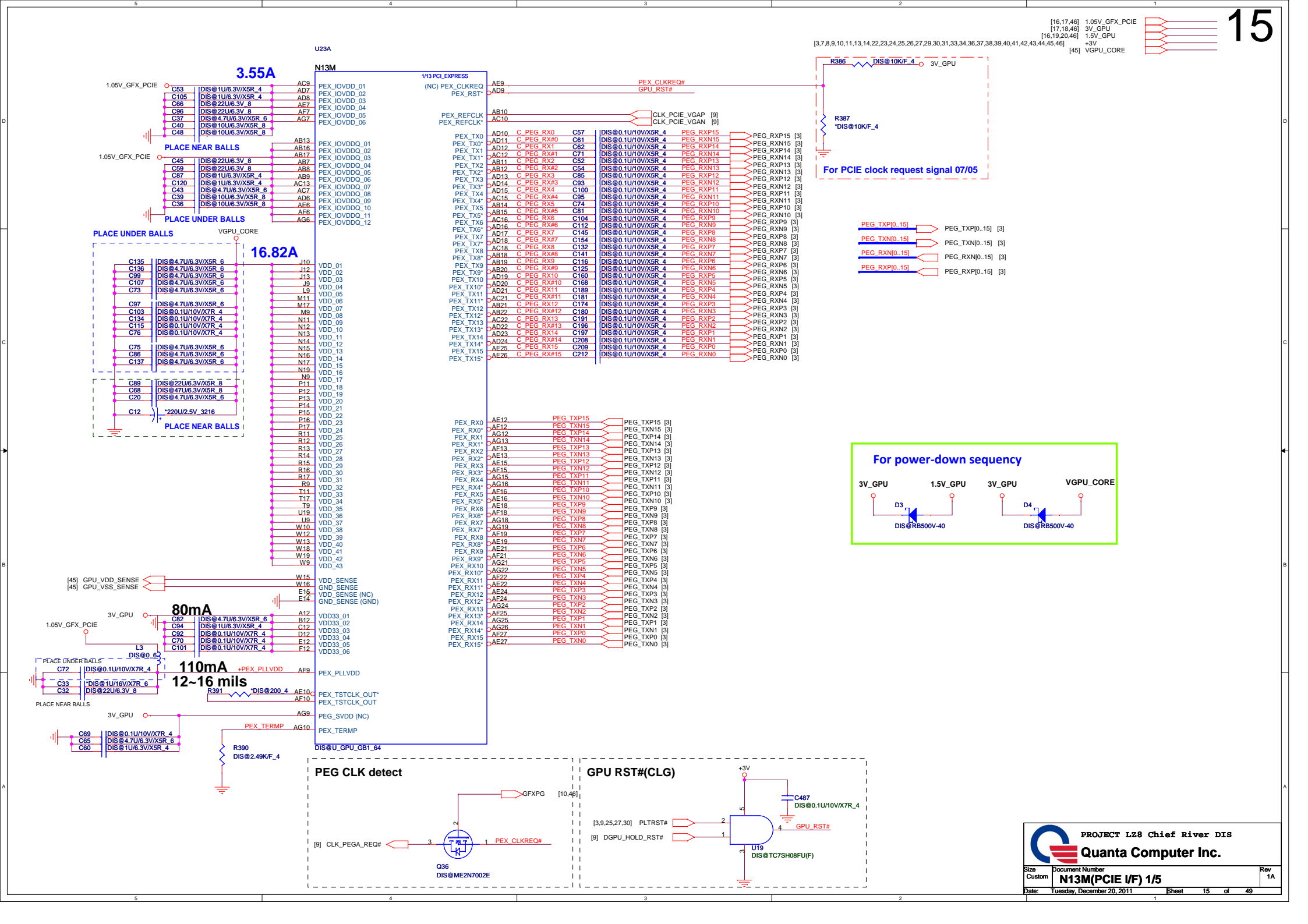


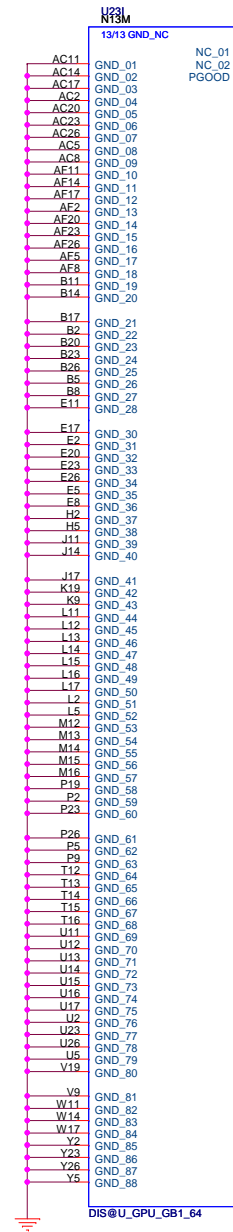
Place these Caps near So-Dimm1.

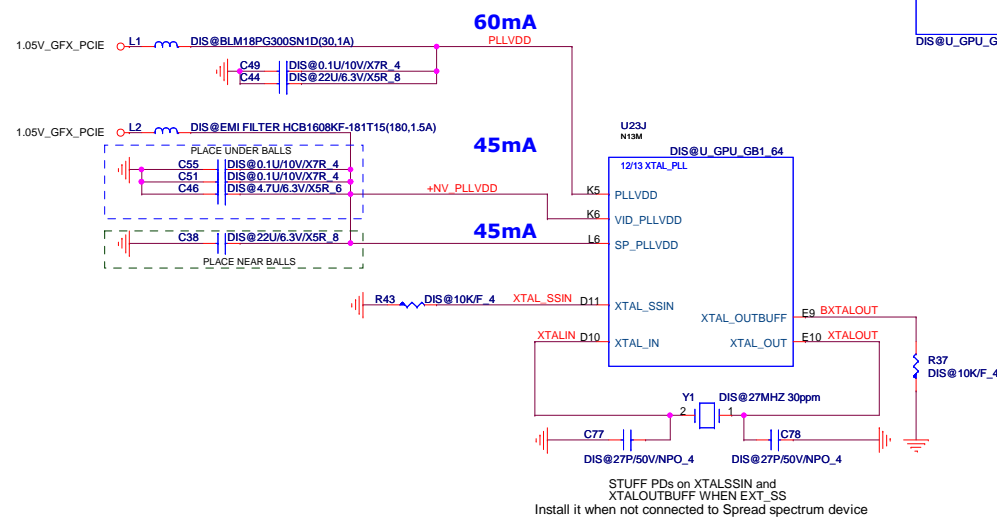
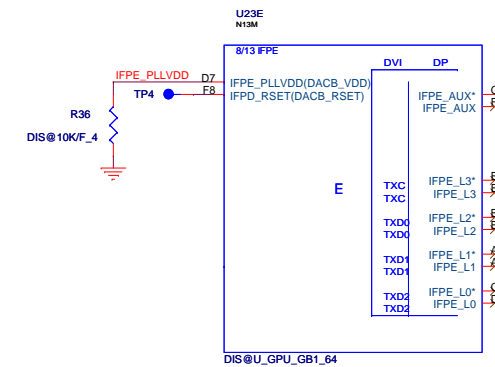
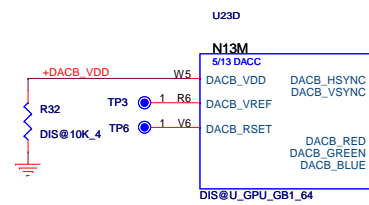
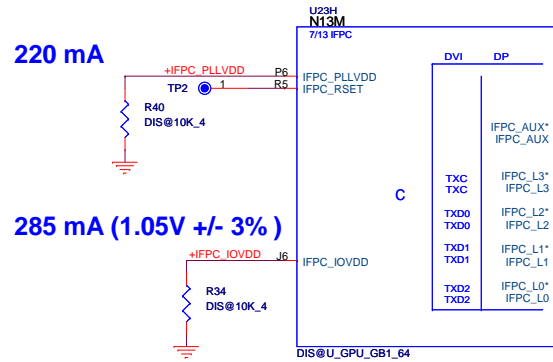
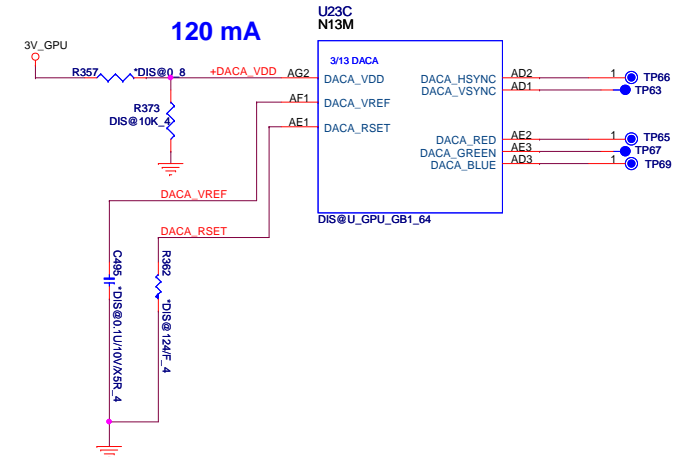
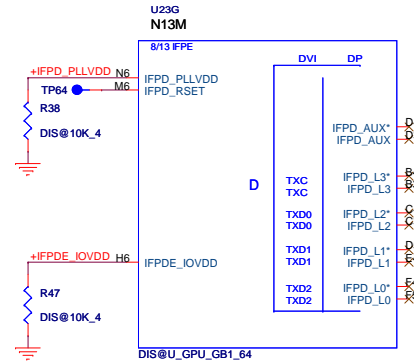
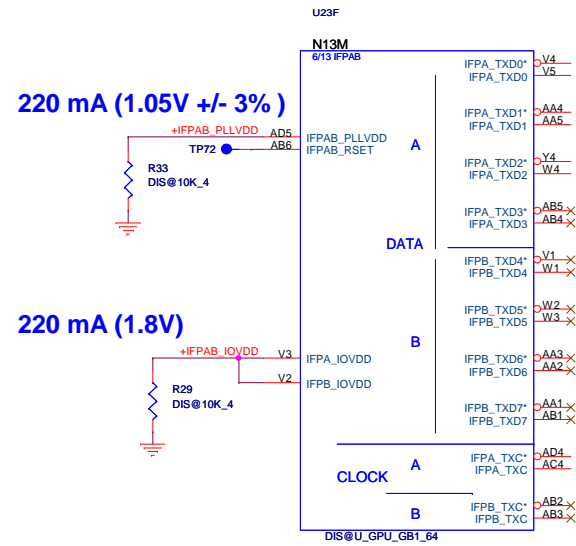


VREF DQ1 M1/M3 Solution



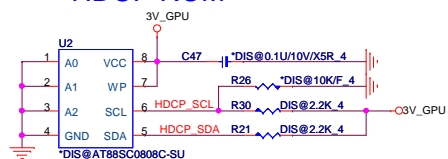








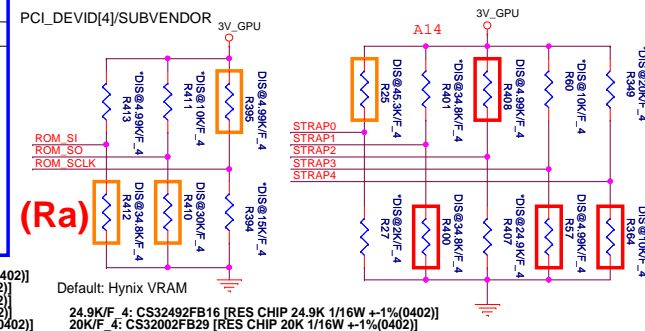
For unused dedicated (non-AUX) I2C pins, pull-up both the I2Cx_SCL, I2Cx_SDA, to 3.3 V using 2.2 kΩ resistors, routing.



DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

Logical Strap Bit Mapping		
Rv	PU-VDD	PD-GM
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

N13M-GE1

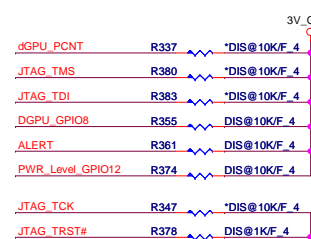


	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO N13M-GE1	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	010
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVIDE[5]	PEX_PLL_EN_TERM	101
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	011
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	011
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	100
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	000
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V	000

VRAM Configuration Table

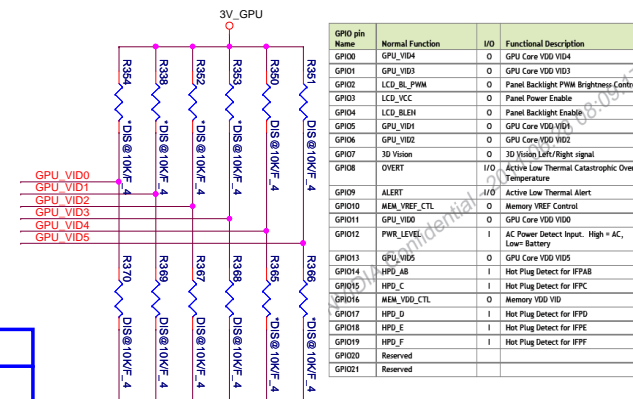
(Ra)	RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_S1
AKD5MGWTTW00 AKD5MGWTT500	0000		Reserved		
	0001		Reserved		
	0010		Reserved		
	0011		Reserved		
	0101		Reserved		
	0110		Reserved		
	0110	DDR3 128Mx16x4, 64bit, 1GB,900MHz	Hynix	H5TQ2G63BFR-11C	PD 34.8K/F
	0111	DDR3 128Mx16x4, 64bit, 1GB,900MHz	Samsung	K4W2G1646C-HC11	PD 45.3K/F

(Ra)



NVVDD Table

N13M-GE1 (GF119)	NVVDD (0.875V)
GPU_VID0	0 (R370)
GPU_VID1	0 (R369)
GPU_VID2	0 (R367)
GPU_VID3	0 (R368)
GPU_VID4	1 (R350)
GPU_VID5	1 (R351)

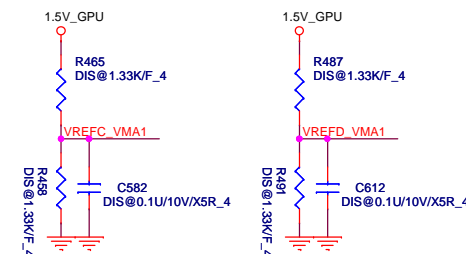
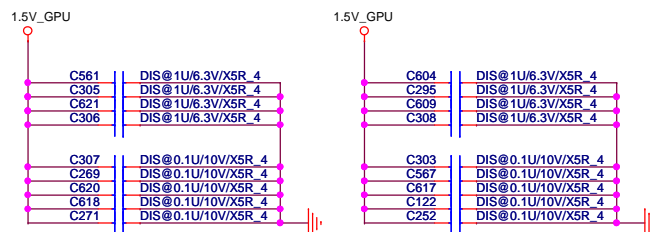
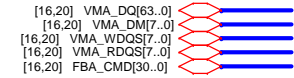
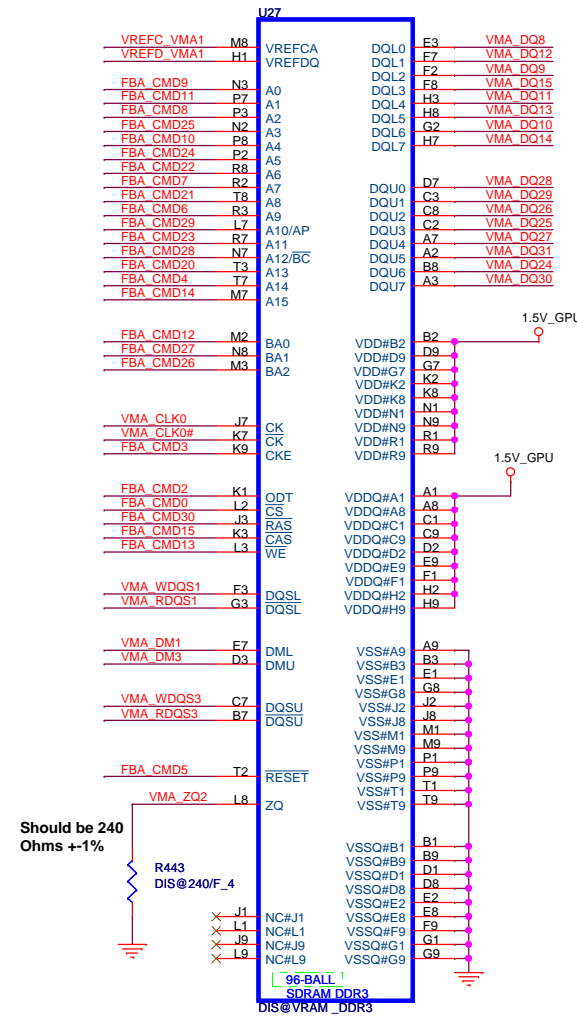
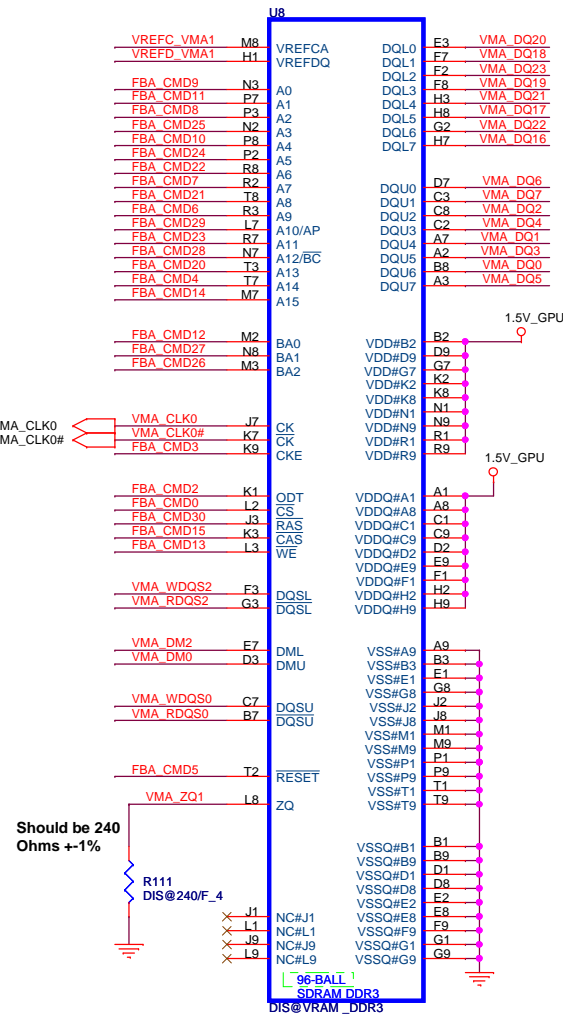


GPID pin name	Normal Function	I/O	Functional Description
GPIO0	GPU_VDD0	0	GPU Core VDD VDD0
GPIO1	GPU_VDD3	0	GPU Core VDD VDD3
GPIO2	LCU_BB_PWM	0	Panel Backlight PWM Brightness Control
GPIO3	LCU_BB_LEDEN	0	Panel Backlight Enable
GPIO4	LCU_BB_LEDEN	0	Panel Backlight Enable
GPIO5	GPU_VDD1	0	GPU Core VDD VDD1
GPIO6	GPU_VDD2	0	GPU Core VDD VDD2
GPIO7	3D Vision	0	3D Vision/Light/Sight
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over-Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	0	Memory VREF Control
GPIO11	GPU_VDD0	0	GPU Core VDD VDD0
GPIO12	PWR_LEVEL_CTL	0	AC Power Detect Input. High = AC, Low Battery
GPIO13	GPU_VDD5	0	GPU Core VDD VDD5
GPIO14	GPIO_AB	1	Hot Plug Detect for IPAB
GPIO15	HPO_C	1	Hot Plug Detect for IPFC
GPIO16	MEM_VDD_CTL	0	Memory VDD VDD
GPIO17	HPO_D	1	Hot Plug Detect for IPFD
GPIO18	HPO_E	1	Hot Plug Detect for IPFE
GPIO19	HPO_F	1	Hot Plug Detect for IPFF
GPIO20	GPIO20	Reserved	
GPIO21	Reserved		

CHANNEL A: 1024MB DDR3

[15,16,20,46] 1.5V_GPU

19

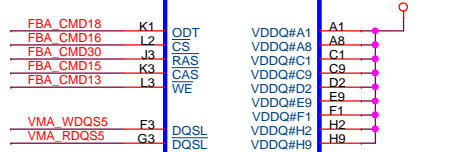
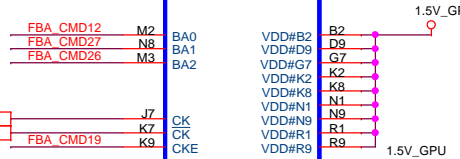
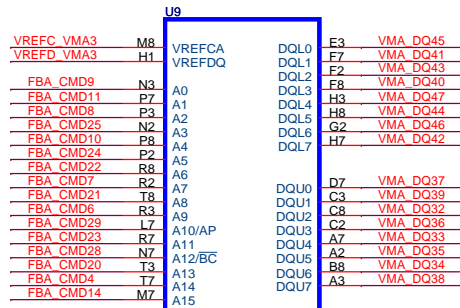


CHANNEL A: 1024MB DDR3

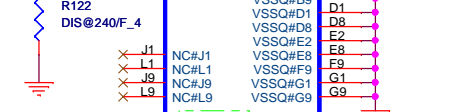
[15,16,19,46] 1.5V_GPU

20

[16,19] VMA_DQ[63..0]
[16,19] VMA_DM[7..0]
[16,19] FBA_CMD[30..0]
[16,19] VMA_RDQS[7..0]

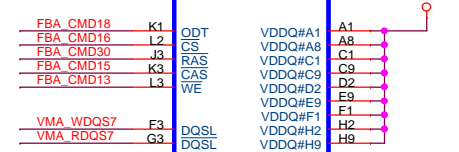
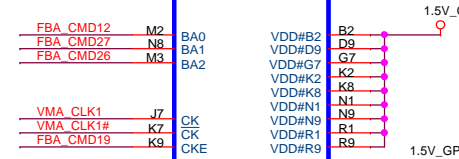
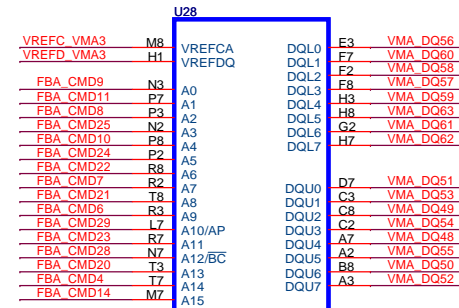


Should be 240 Ohms +1%

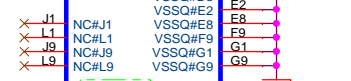


Should be 240 Ohms +1%

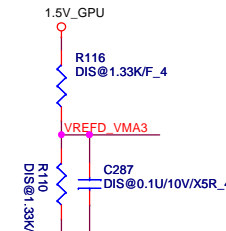
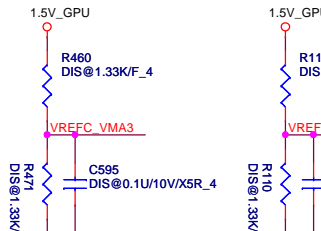
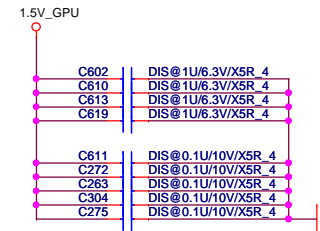
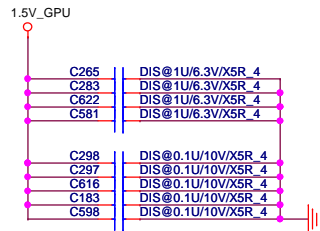
96-BALL
SDRAM DDR3
DIS@VRAM_DDR3



R427 DIS@240/F_4



96-BALL
SDRAM DDR3
DIS@VRAM_DDR3



PROJECT Lz8 Chief River DIS
Quanta Computer Inc.

Size Custom Document Number **N13M (DDR3) 6/6** Rev 1A

Date: Tuesday, December 20, 2011 Sheet 20 of 49

D

D

C

C

B

B

A

A

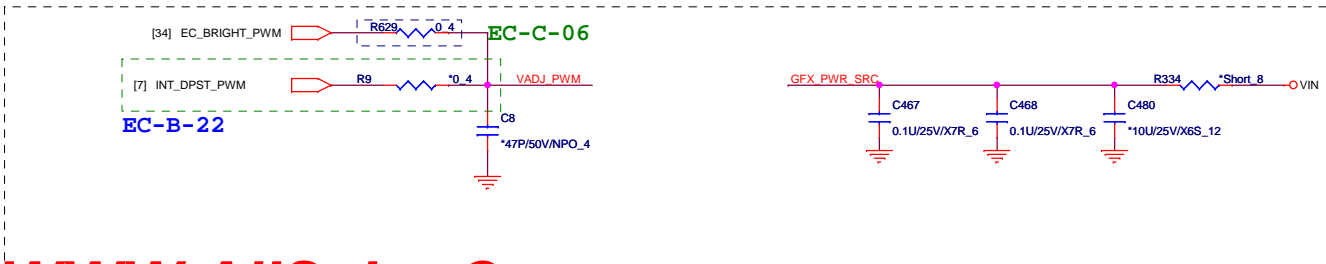
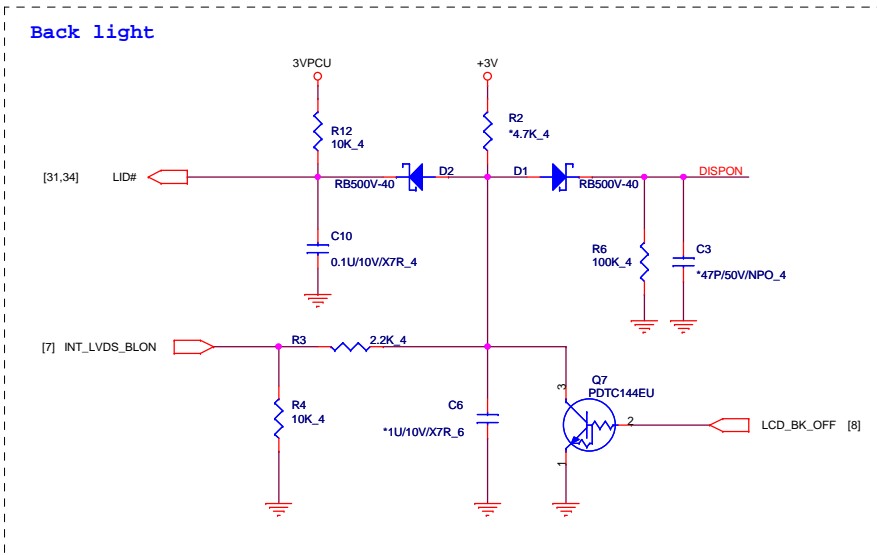
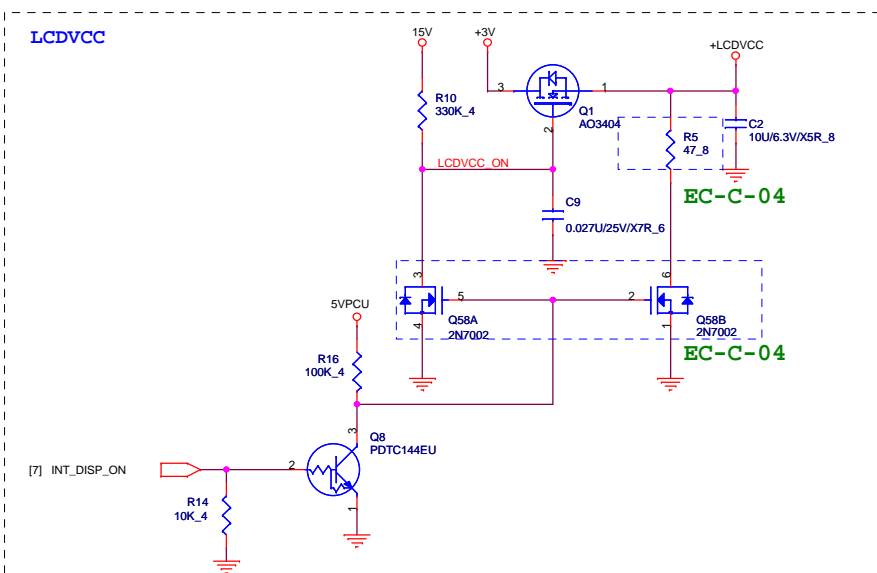


PROJECT LZ8 Chief River DIS

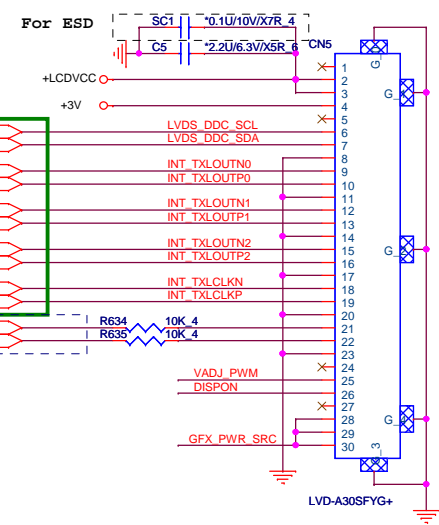
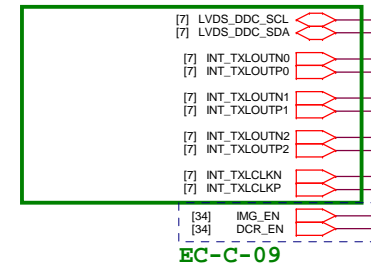
Quanta Computer Inc.

Size Custom	Document Number Blank	Rev 1A
Date: Friday, November 11, 2011	Sheet 21 of 49	1

+3V	[3,7,8,9,10,11,13,14,15,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]
3VPCU	[7,8,25,30,31,34,35,36,37,38,39,43,45]
15V	[37,39,40,46]
VIN	[36,38,39,40,41,42,44,45]
5VPCU	[11,36,37,39,40,41,42,43,44,45,46]

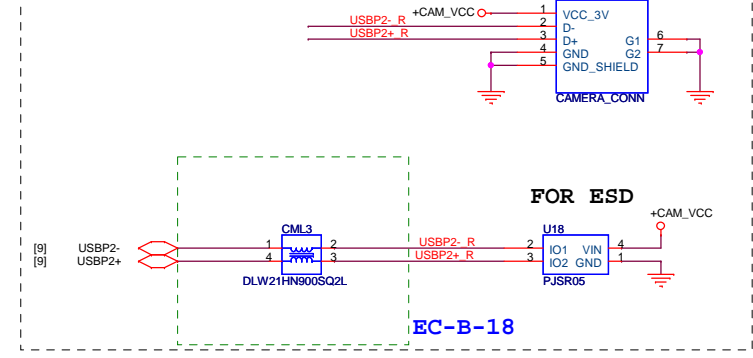


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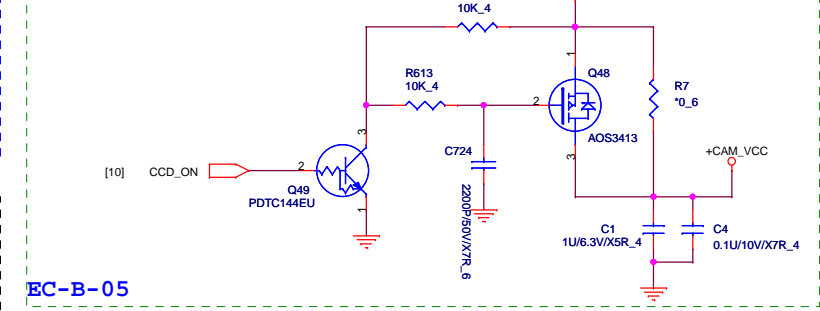


LVDS (14")
(1024x600,
1366x768)

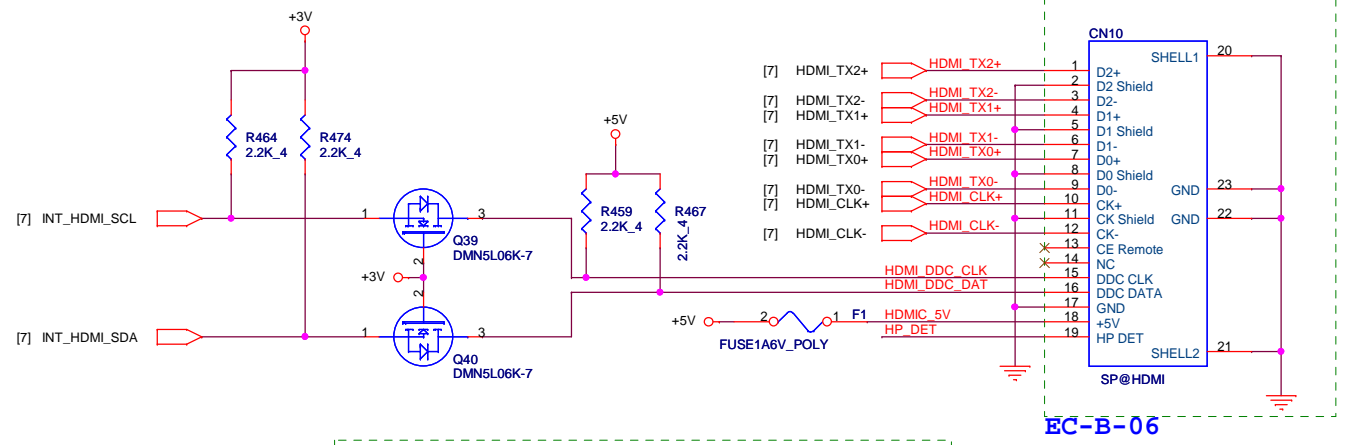
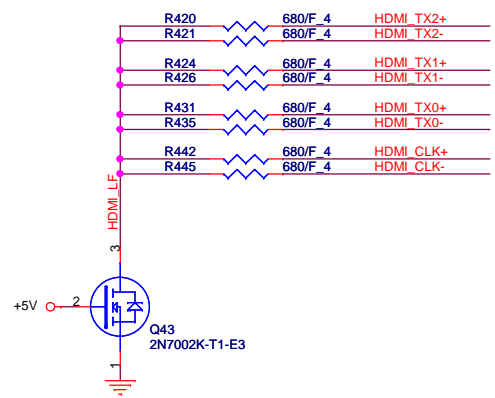
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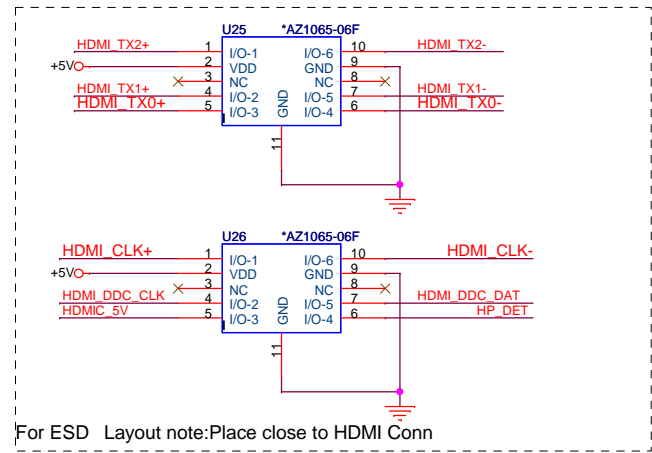
CAMERA VCC Control



[3,7,8,9,10,11,13,14,15,22,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46] +3V
[8,11,24,26,33,36,37,38] +5V

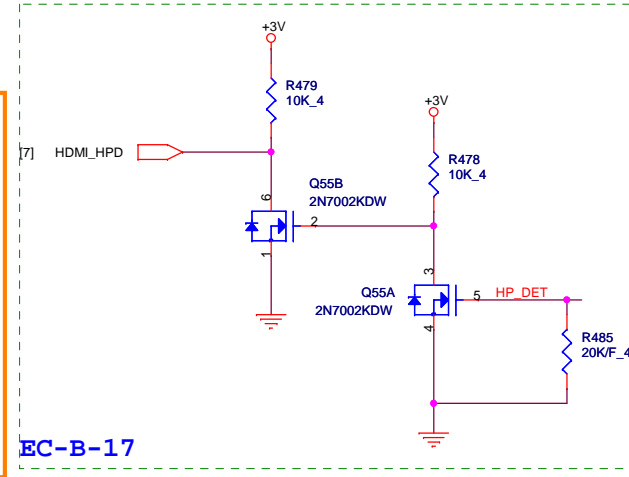
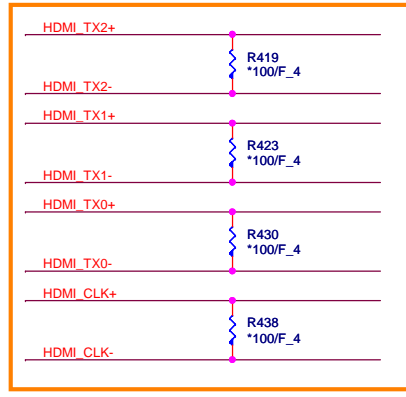


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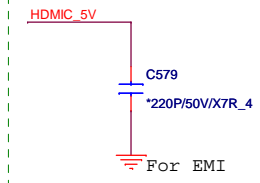


For ESD Layout note: Place close to HDMI Conn

EMI reserve for HDMI



EC-B-17

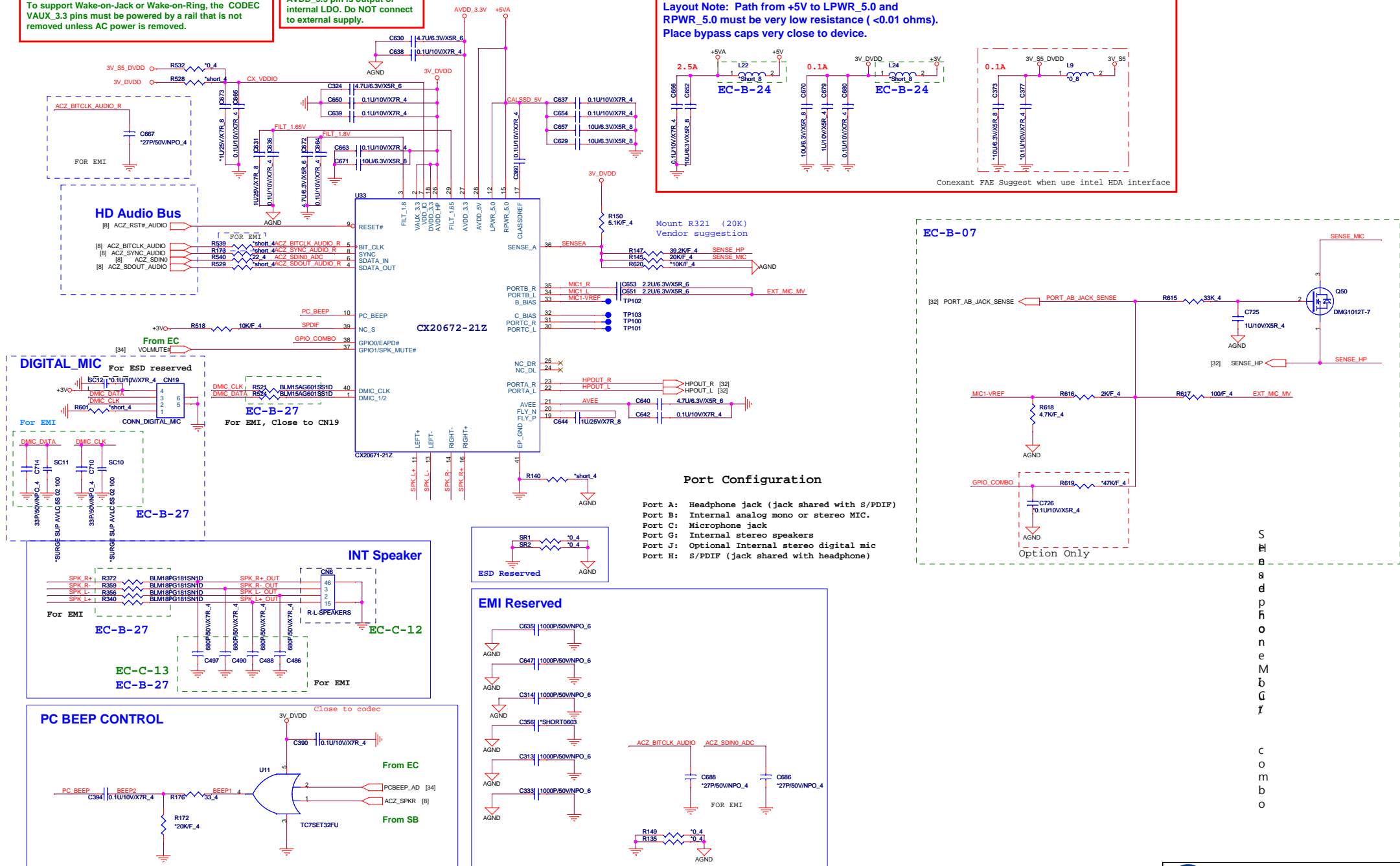


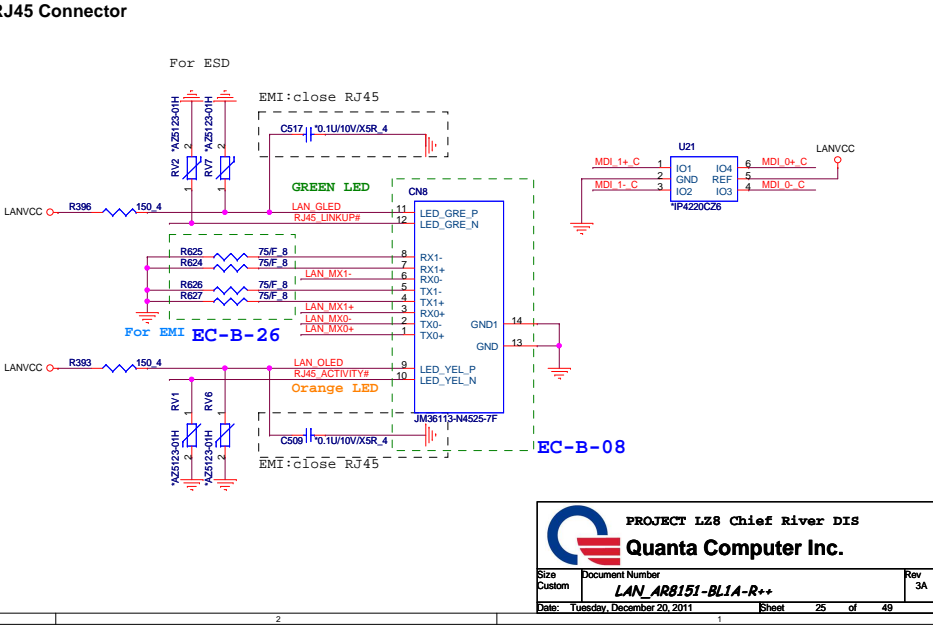
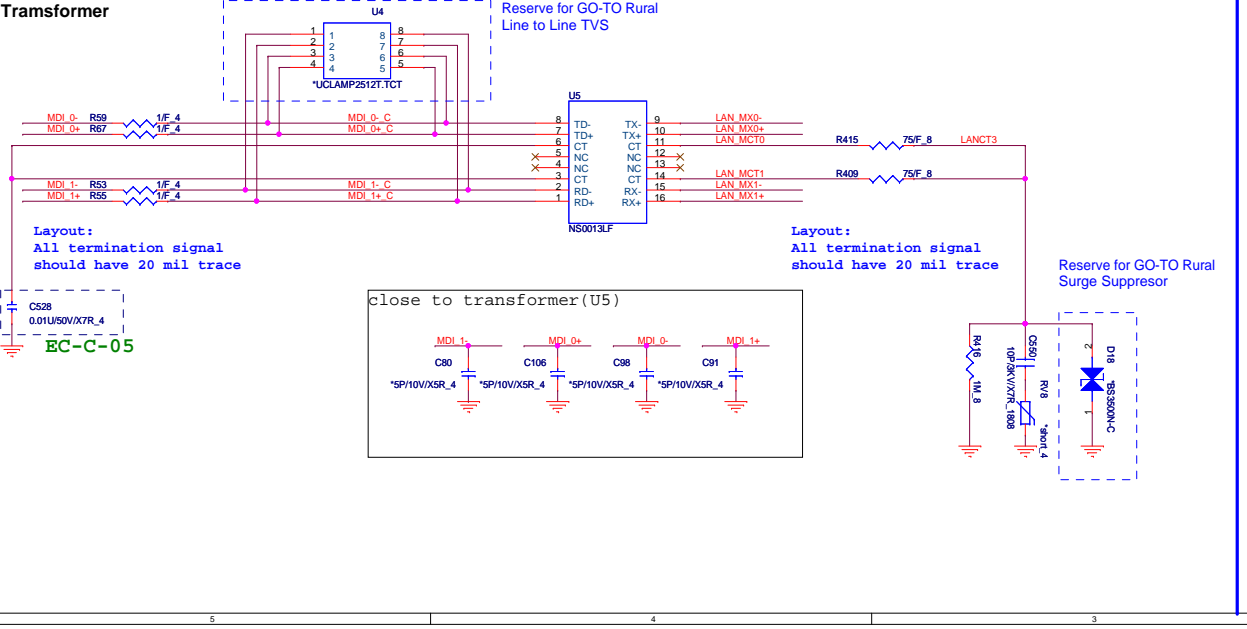
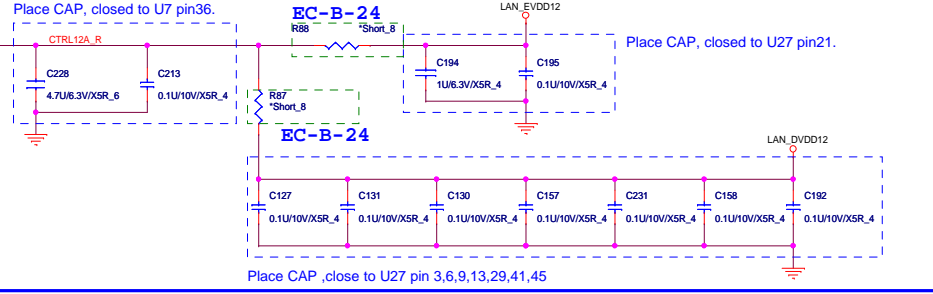
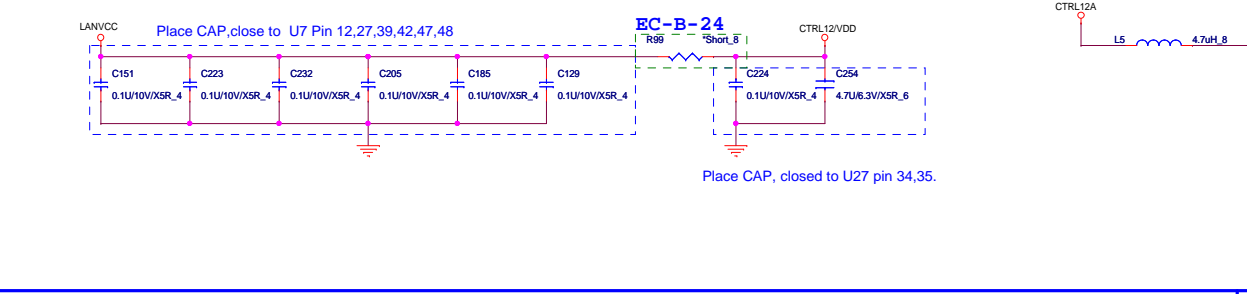
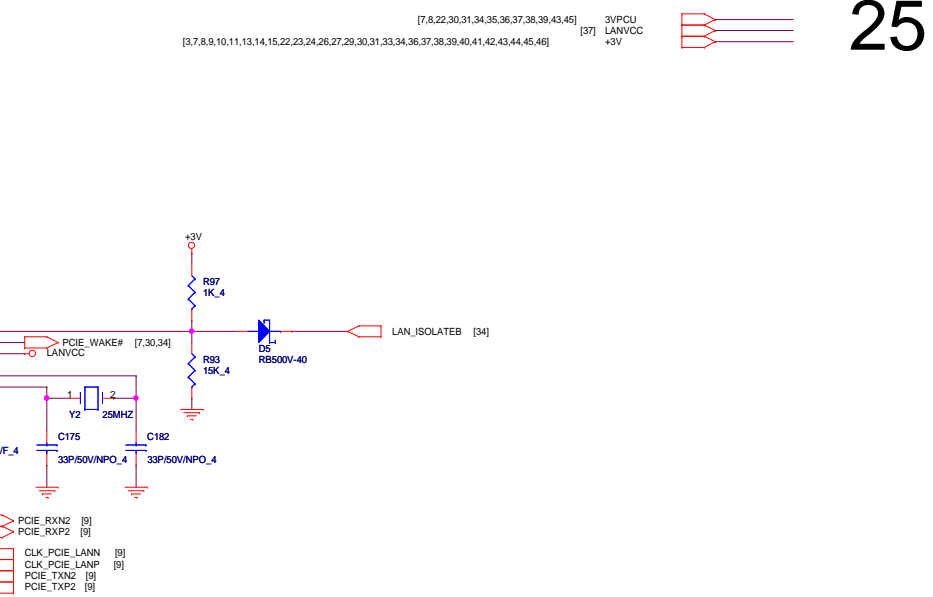
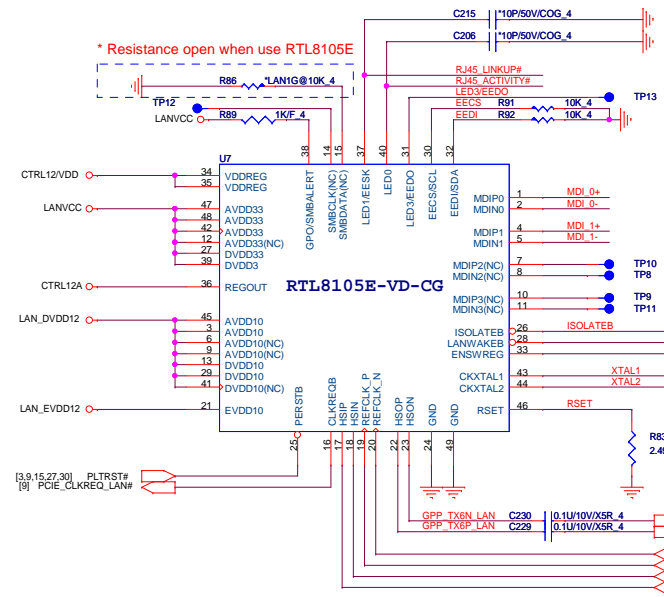
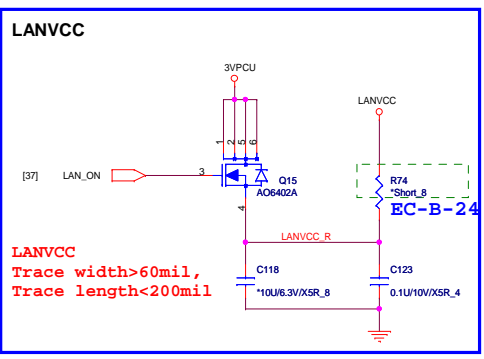
Note:

To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 pins must be powered by a rail that is not removed unless AC power is removed.

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

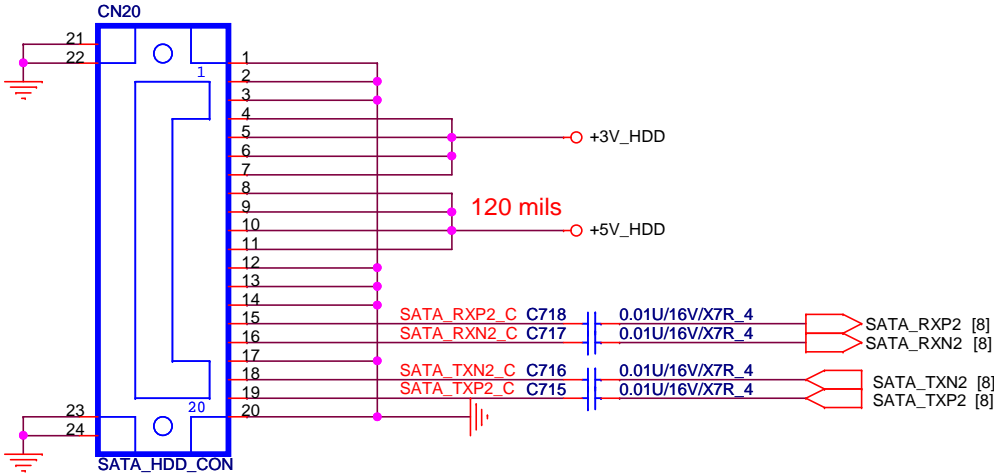
Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.



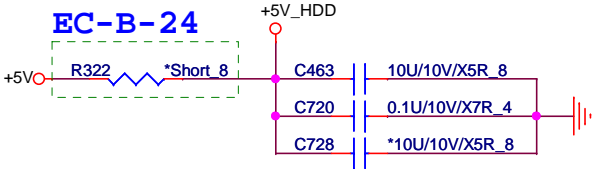


PLACE SATA AC COUPLING
CAPS CLOSE TO Connector

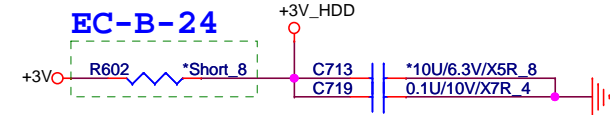
+3V [3,7,8,9,10,11,13,14,15,22,23,24,25,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]
+5V [8,11,23,24,33,36,37,38]

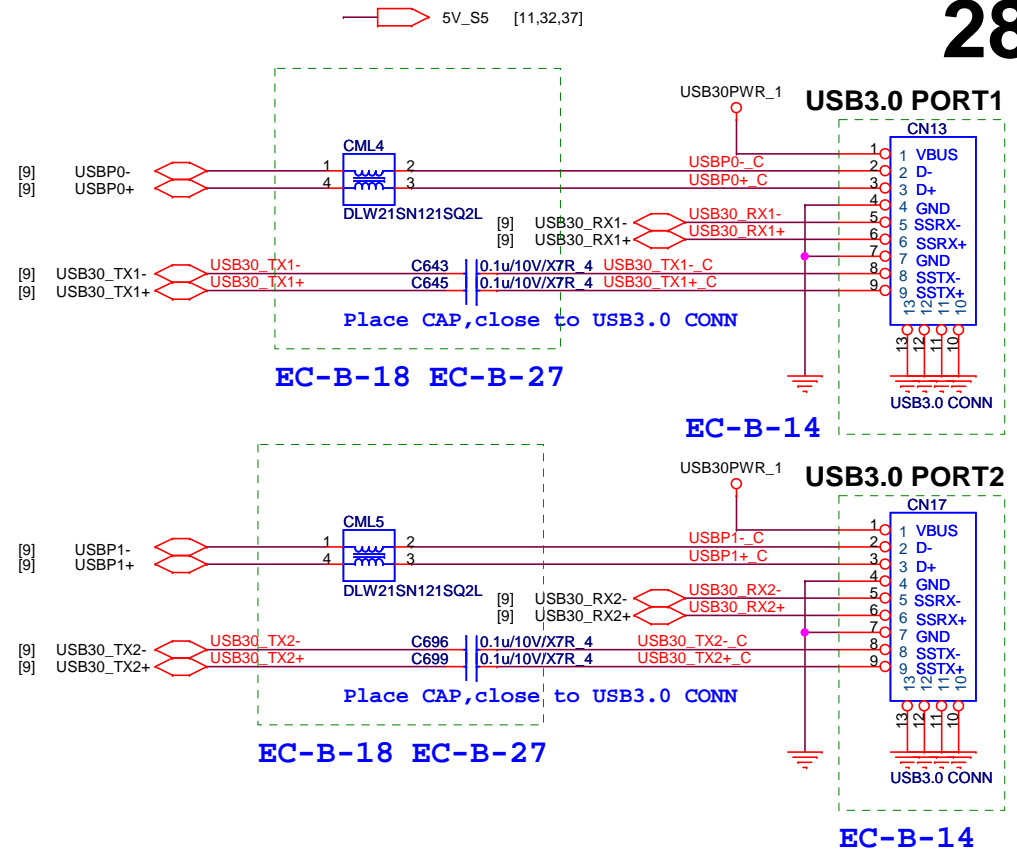
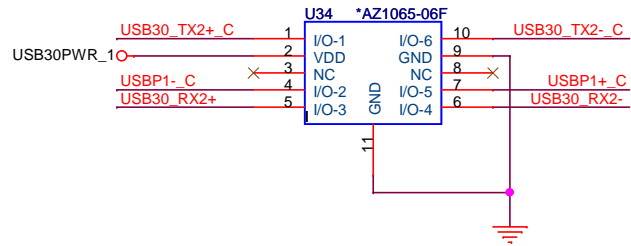
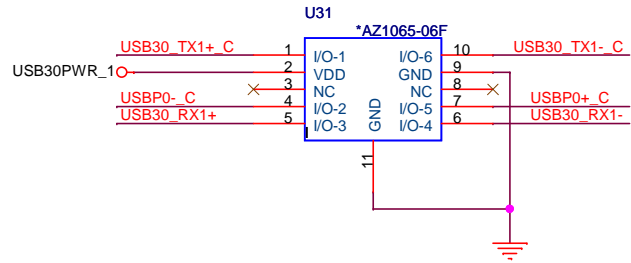
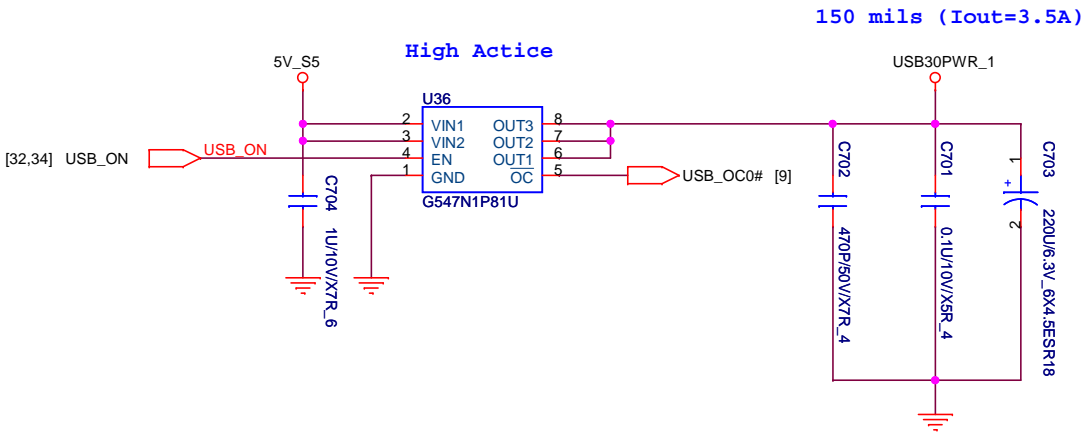


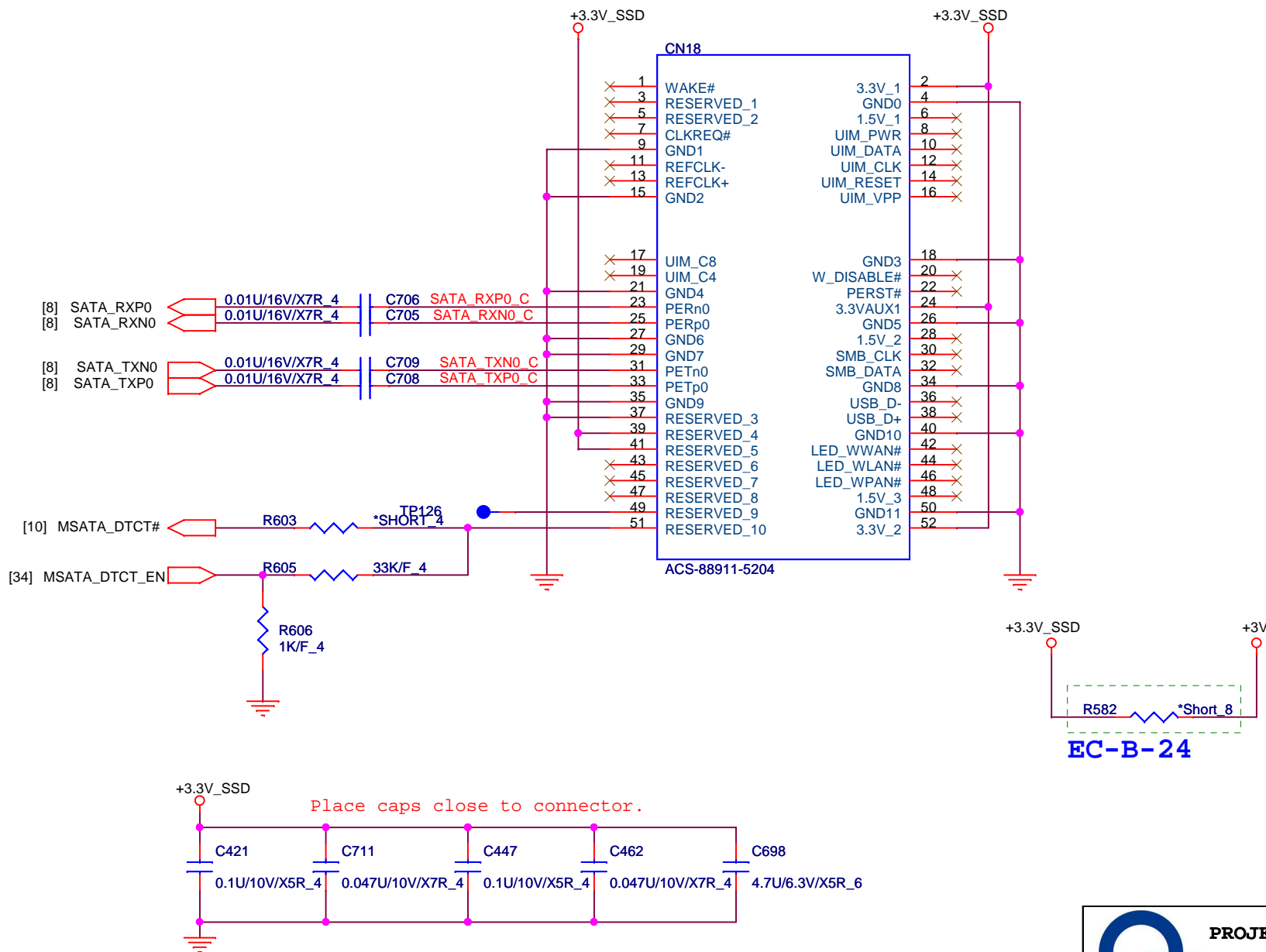
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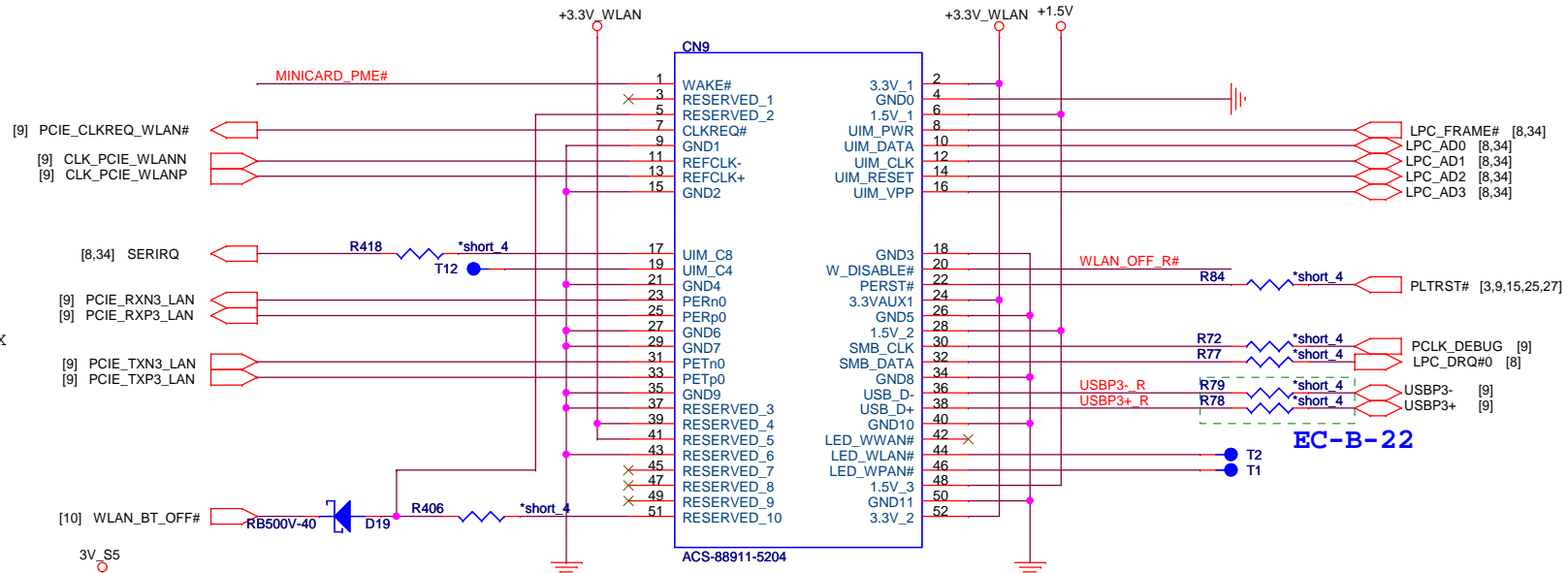
DC Current rating: 3 A (MAX)





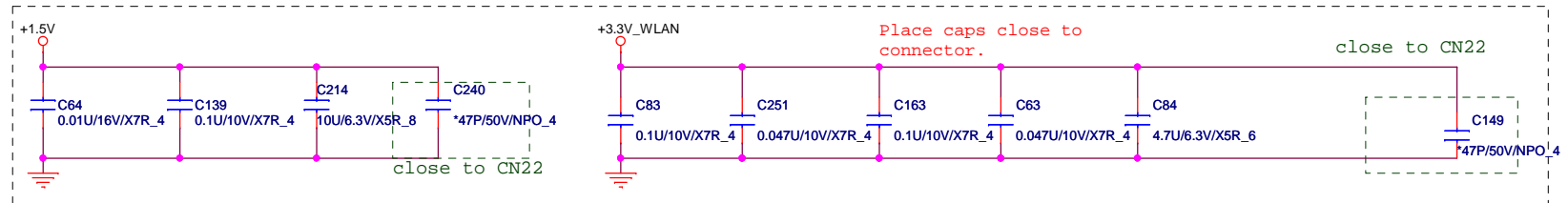


MiniCard WLAN connector

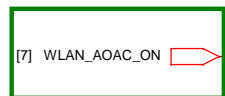


PCI-Express TX and RX
direct to connector

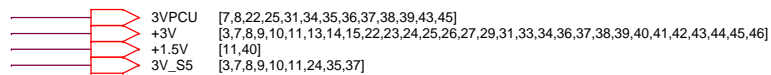
FOR DEEP S3 EC-B-01

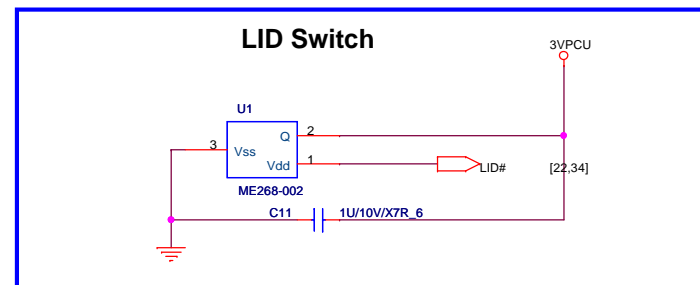
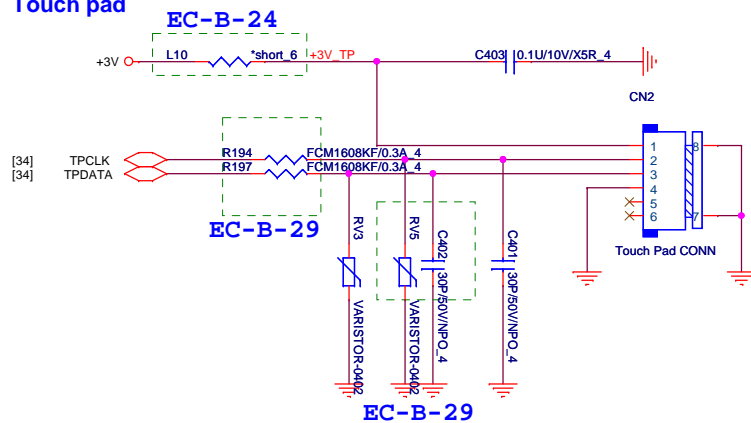


AOAC

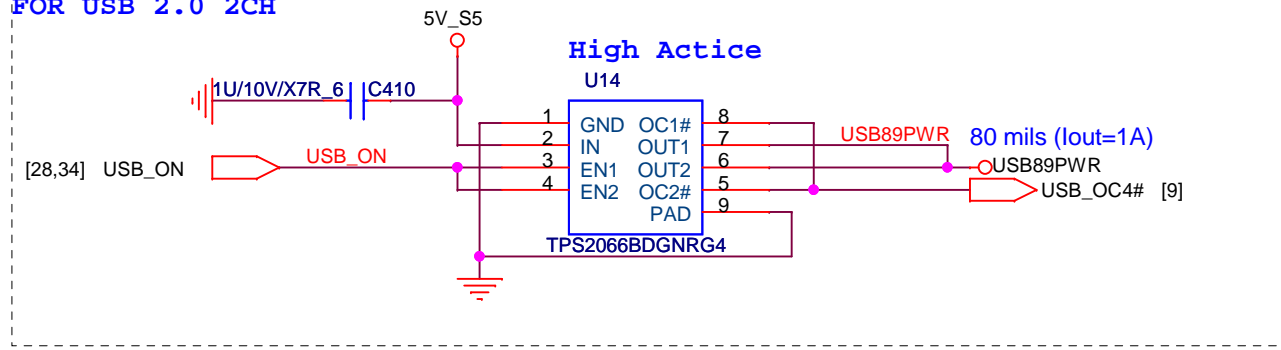


EC-B-13

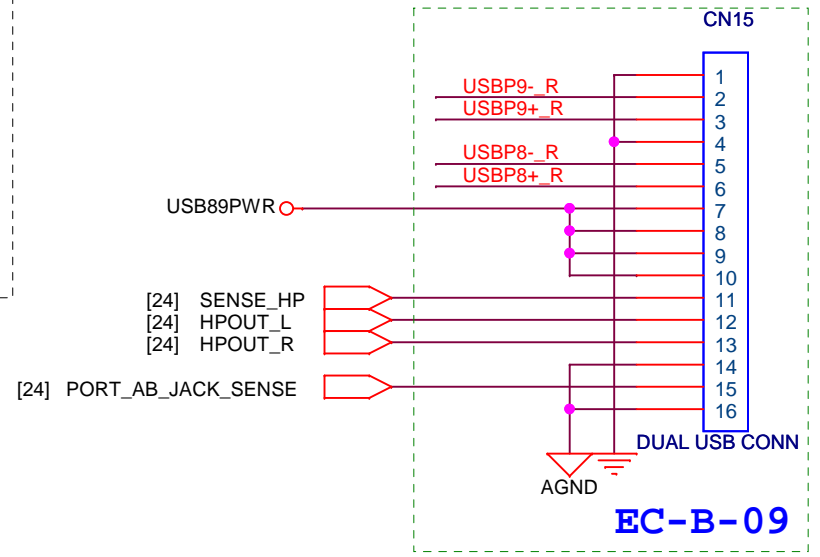




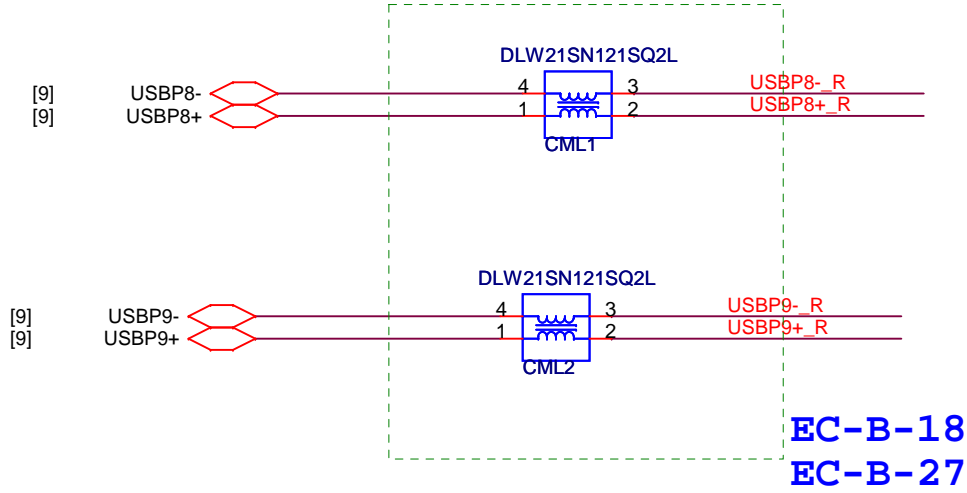
FOR USB 2.0 2CH




5V_S5 [11,28,37]



EC-B-09

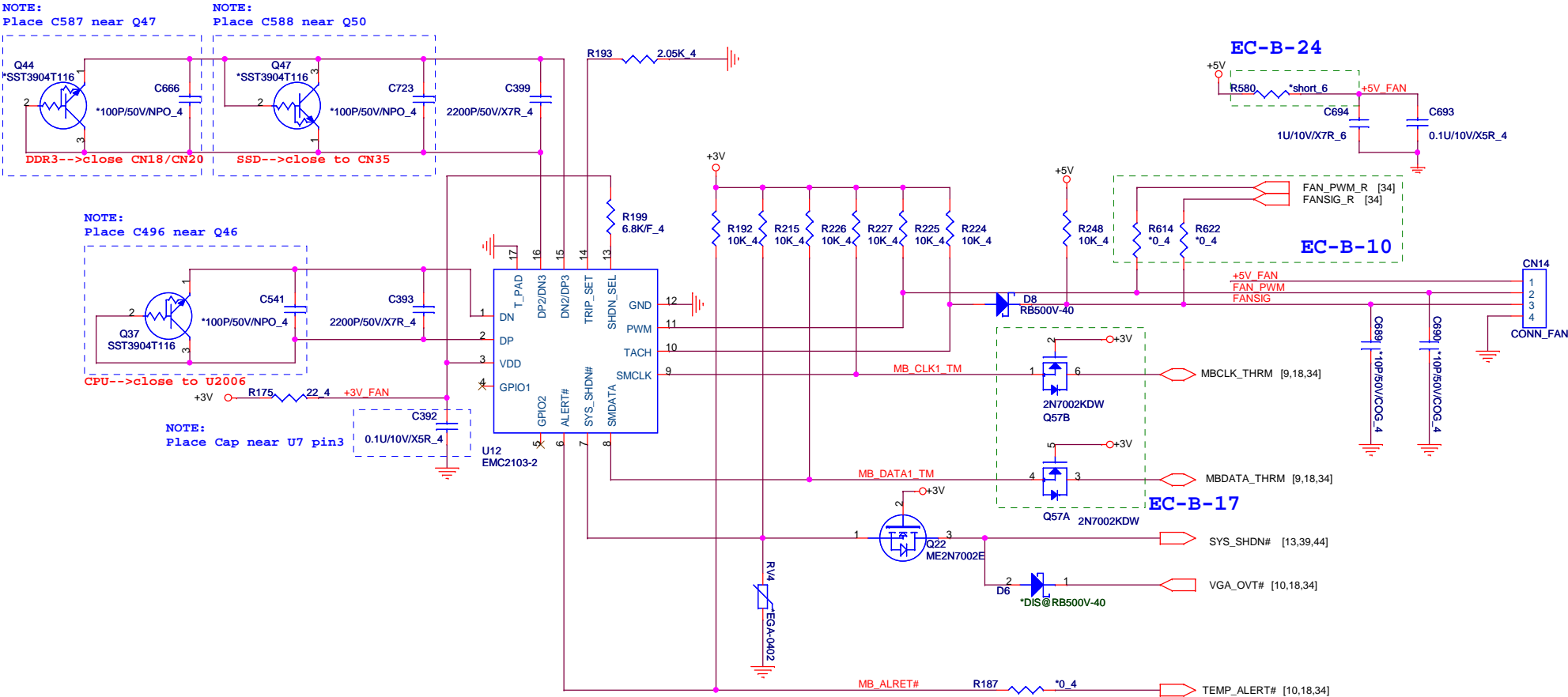


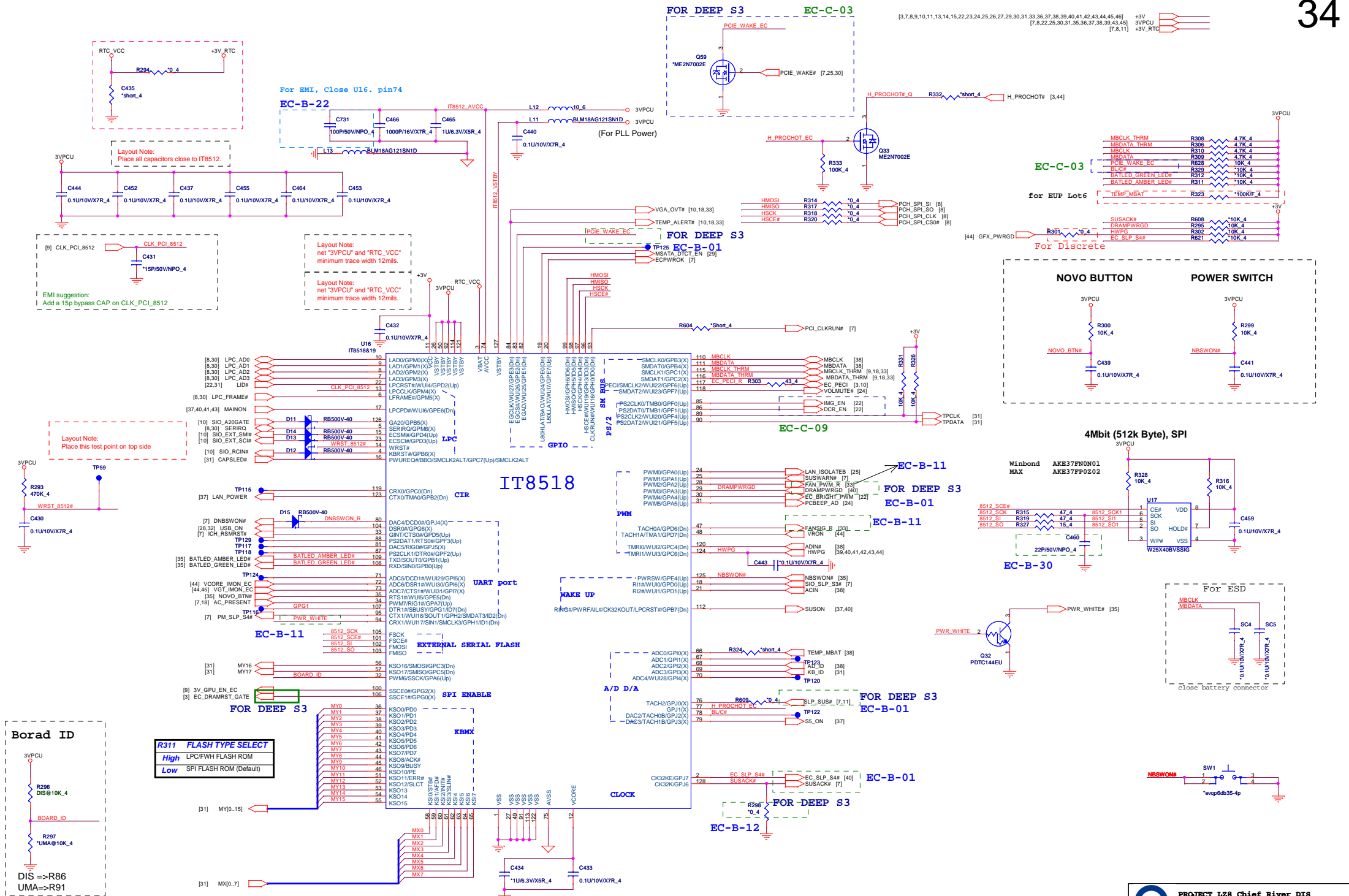


PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

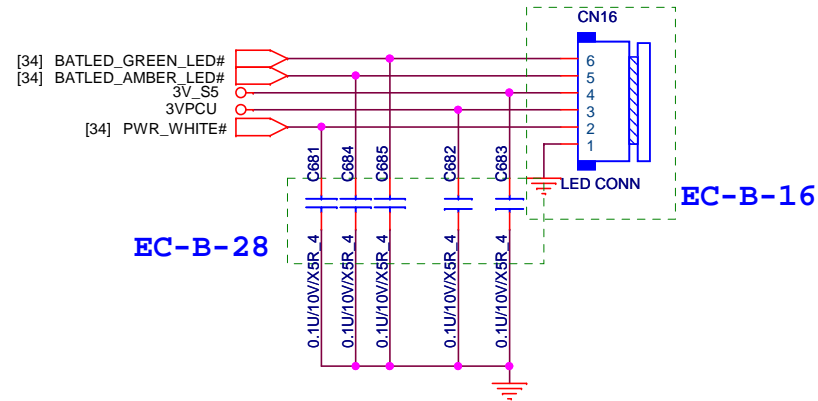
Size	Document Number	Rev
	USB2.0--Audio Jack Conn	3A
Date:	Tuesday, December 20, 2011	Sheet 32 of 49



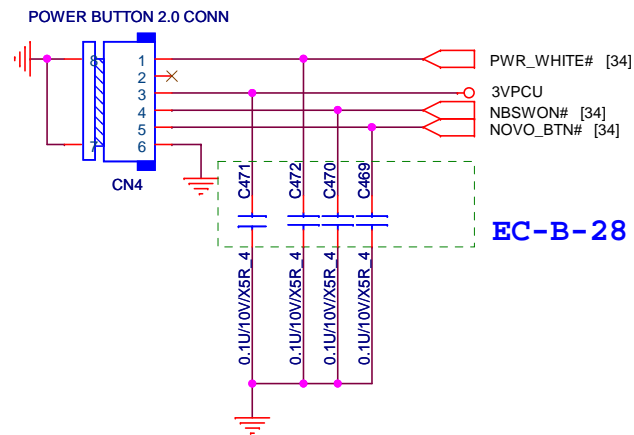


3VPCU [7,8,22,25,30,31,34,36,37,38,39,43,45]
3V_S5 [3,7,8,9,10,11,24,30,37]

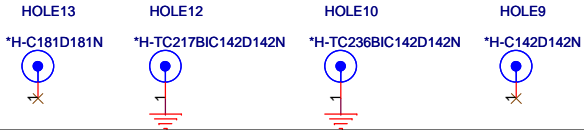
LED Conn



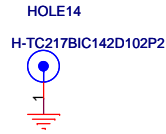
POWER BUTTON/NOVO Button



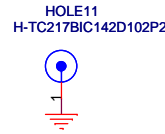
Hole for CPU support



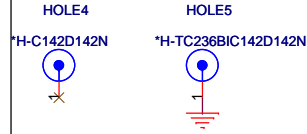
MiniCard WWAN



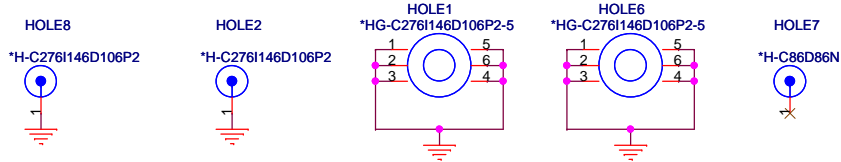
MiniCard WLAN



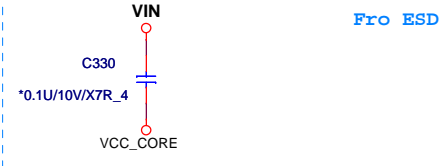
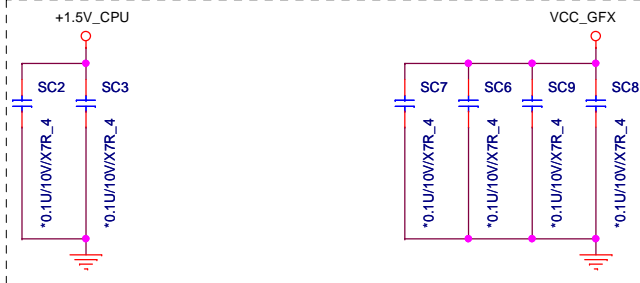
Hole for GPU support



Boundary Hole

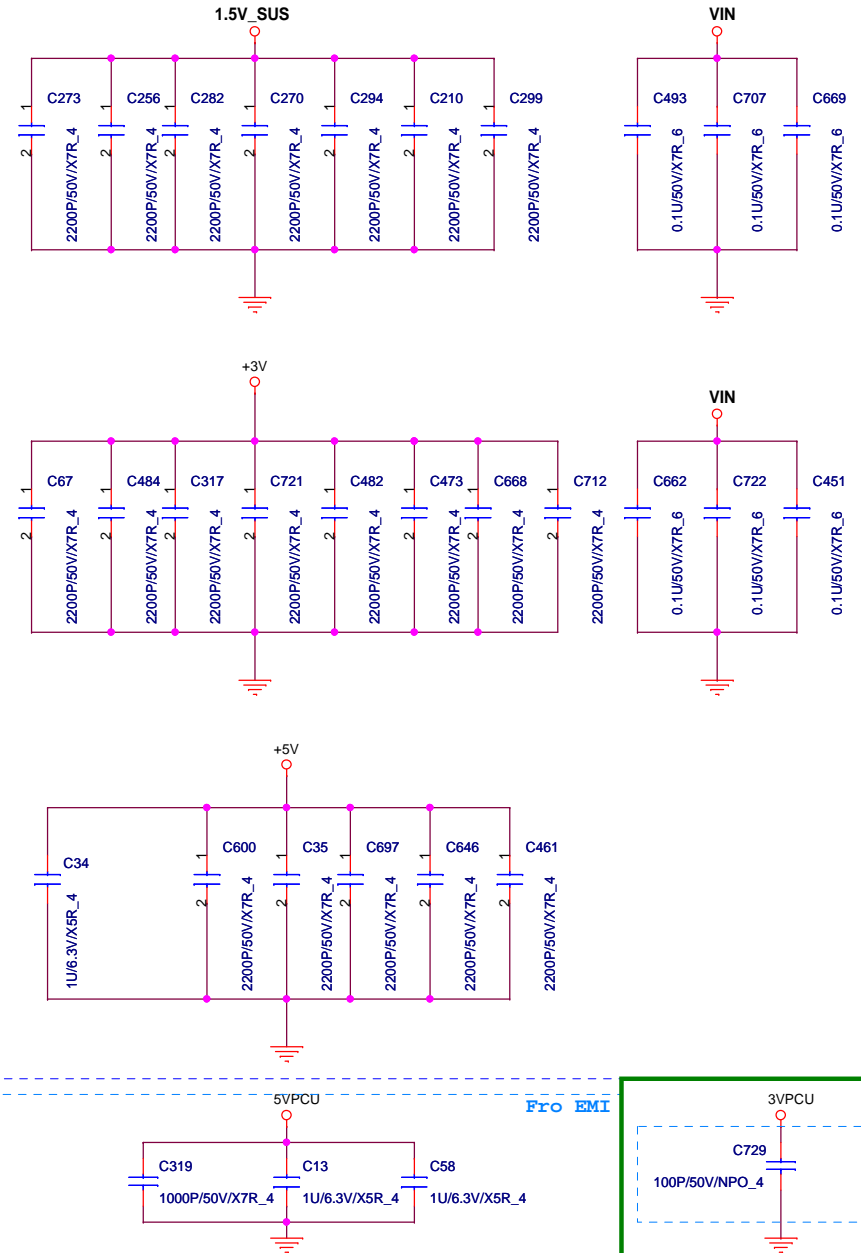


Fro ESD



	+1.5V_CPU	[3,5,40]
	3VPCU	[7,8,22,25,30,31,34,35,37,38,39,43,45]
	VCC_GFX	[5,44]
	+3V	[3,7,8,9,10,11,13,14,15,22,23,24,25,26,27,29,30,31,33,34,37,38,39,40,41,42,43,44,45,46]
	+5V	[8,11,23,24,26,33,37,38]
	1.5V_SUS	[3,11,13,14,37,40,46]
	5VPCU	[11,22,37,39,40,41,42,43,44,45,46]
	VIN	[22,38,39,40,41,42,44,45]
	VCC_CORE	[5,6,44]
	+1.05V	[3,5,7,8,9,11,37,41,46]

EMI

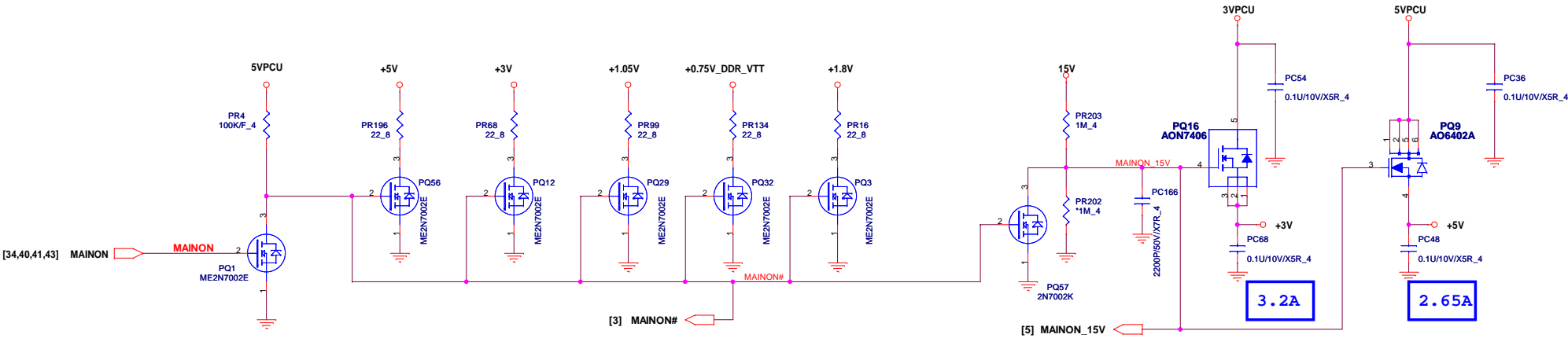


EC-B-22

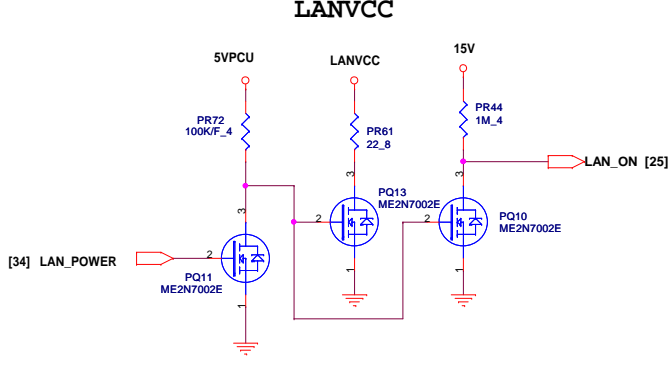
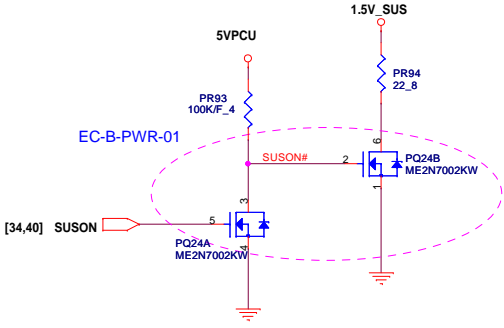
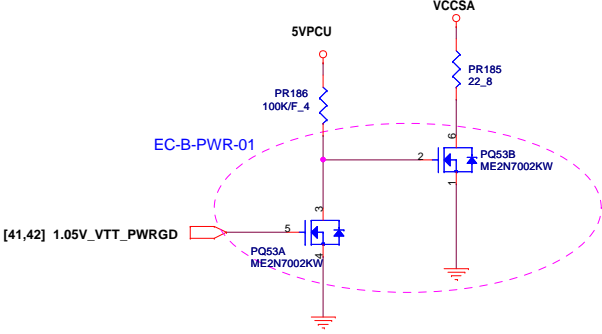
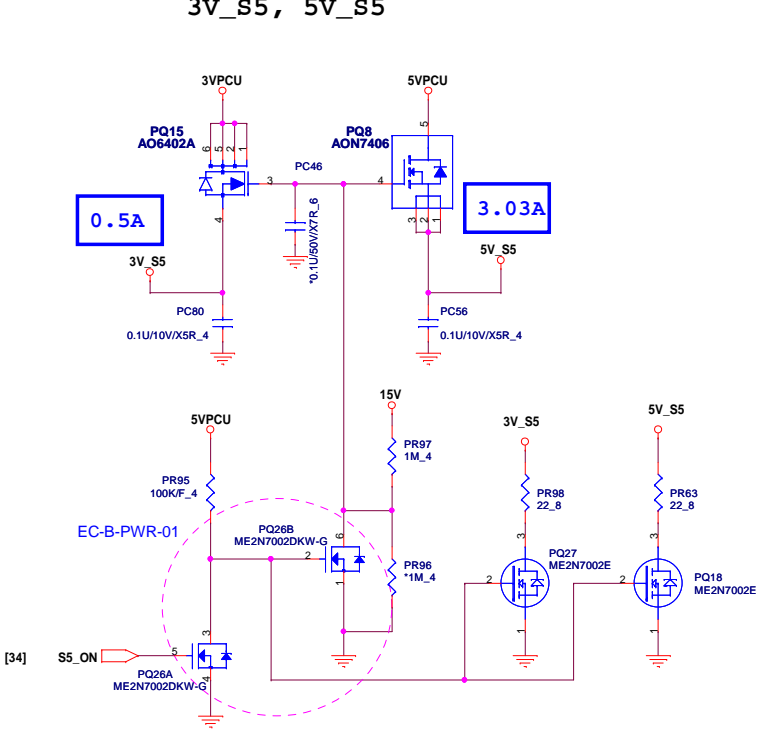
For EMI, Close U16.PIN92

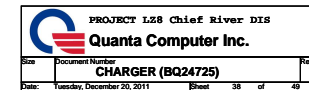
PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

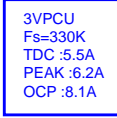
Size	Document Number	Rev
	Screw Hole/EMI	1A
Date:	Tuesday, December 20, 2011	Sheet 36 of 49



3V_S5, 5V_S5

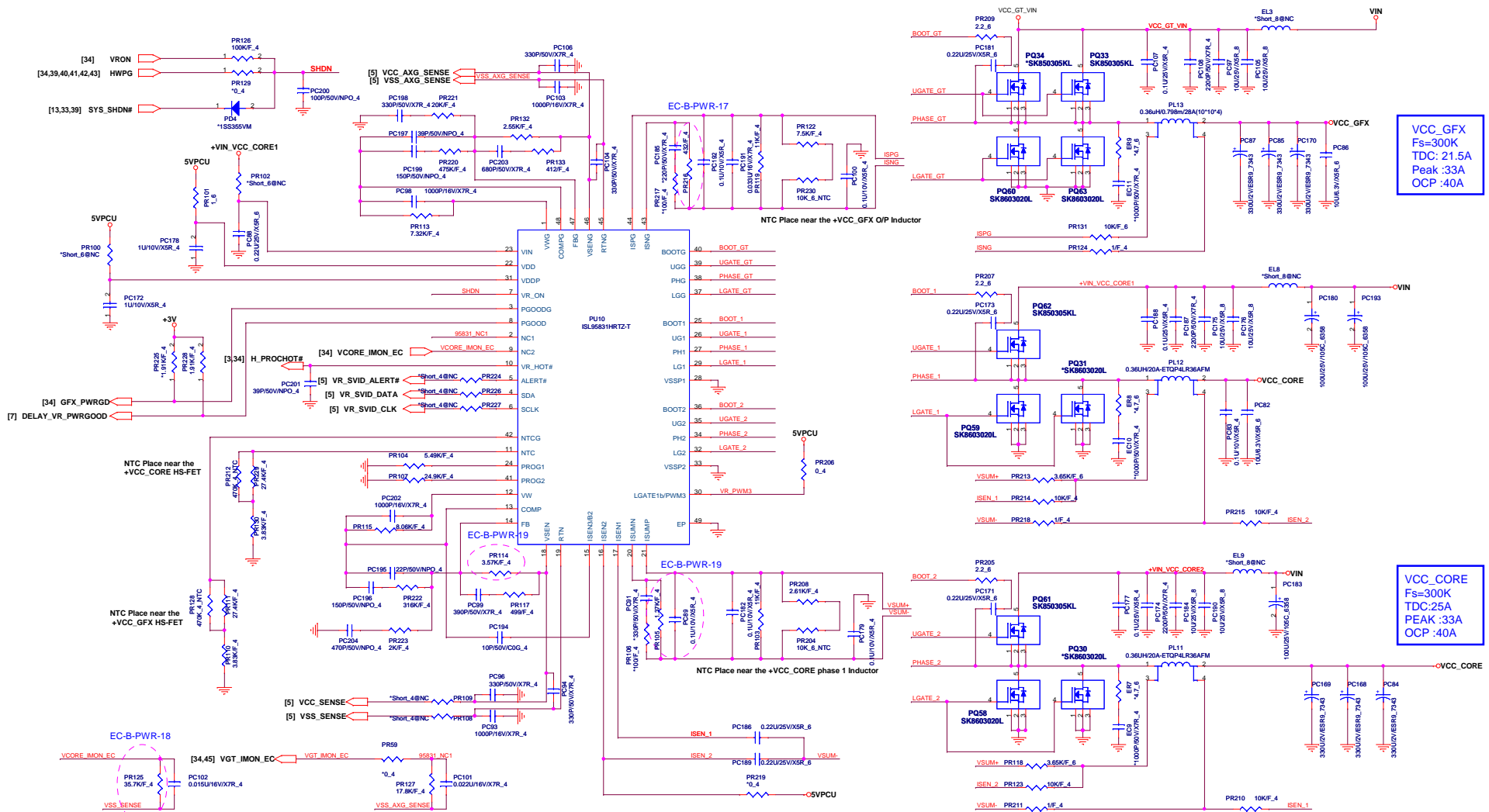


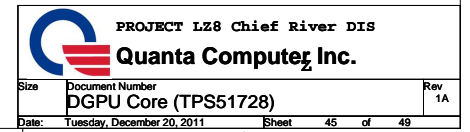


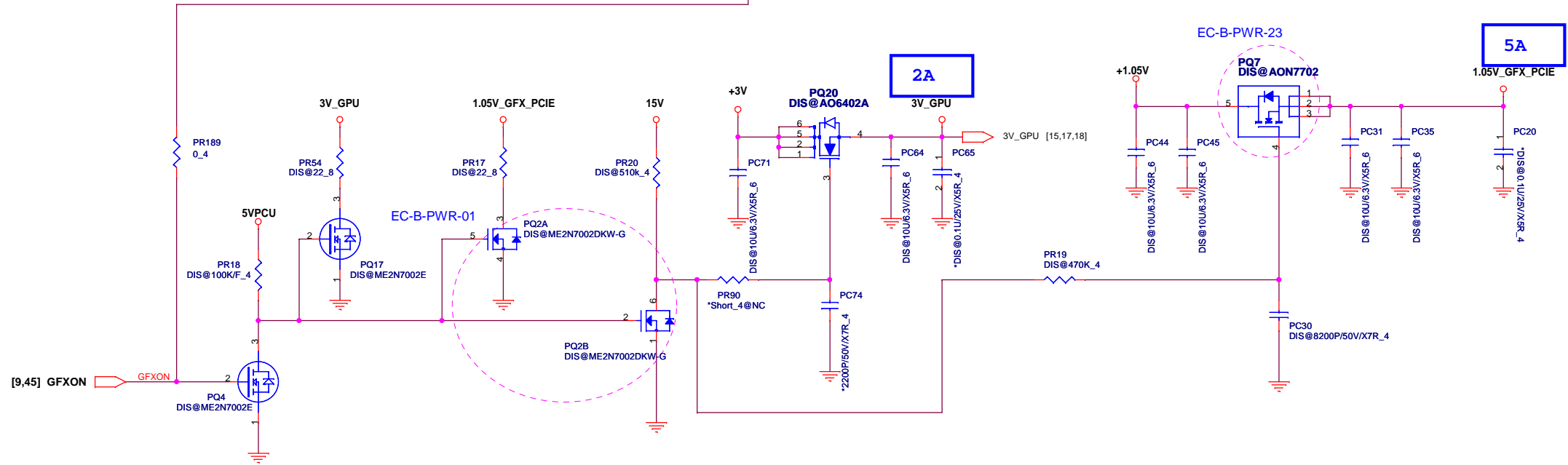
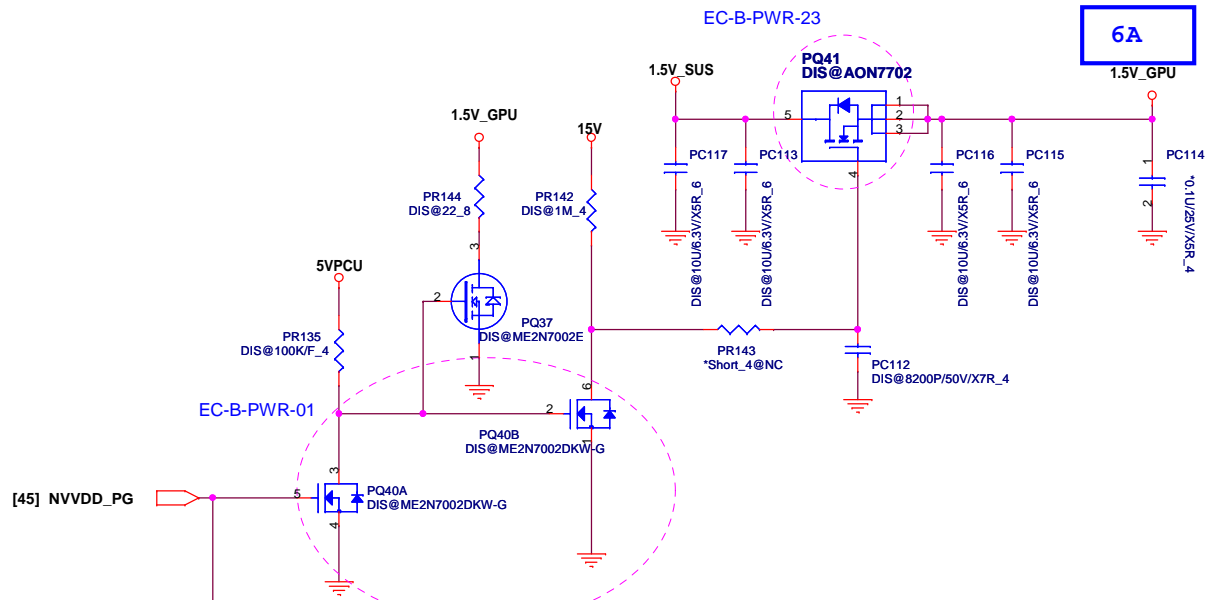
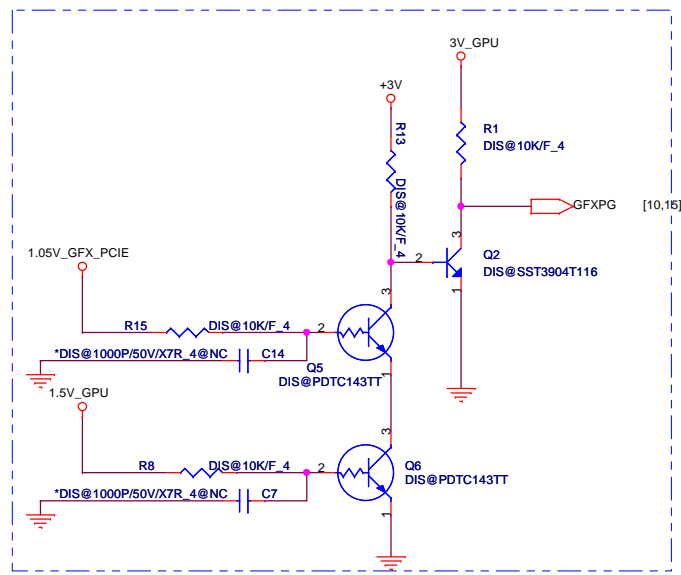


B

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E C N	P G	D A r/mm/dd	P A	D E
EC-B-01	7,11,34	11/10/13	Add R607,R608,R621 and no ASM	Add DEEP S3 function
EC-B-02	7	11/10/13	R210	R210 chnage to short pad
EC-B-03	9	11/10/13	R610 no ASM,R611 ASM, R	For DGPU power enable sequence
EC-B-04	10	11/10/13	R573 no ASM,R572 ASM	Change Board ID for SIV stage
EC-B-05	10,22	11/10/13	R49,R613,C724,R612,Q48 add and ASM	Change CCD control by PCH GPIO35
EC-B-06	23	11/10/13	CN10	Change CN10 to correct footprint
EC-B-07	24	11/10/13	R	Change Audio detect schematic
EC-B-08	25	11/10/13	CN8	Change CN8 to correct footprint
EC-B-09	32	11/10/13	CN15	Change CN25 Pin define
EC-B-10	33	11/10/13	Add R614,R622 no ASM	Add EC detect Fan speed schematic
EC-B-11	34	11/10/13	DEL R321	Change EC pin define,PIN94 connect to PWR_WHITE,PIN28 connect to FAN_PWM_R,PIN47 connect to FANSIG_R
EC-B-12	34	11/10/13	R298 no ASM	EC can output CLOCK by itself
EC-B-13	30	11/10/13	R35 no ASM,Q11ASM	input AOAC function
EC-B-14	28	11/10/13	CN13,CN17	Change CN13,CN17 to correct footprint
EC-B-15	28	11/10/13	add Q51,R623 no ASM	Add DEEP S3 function
EC-B-16	35	11/10/13	CN16	Change CN16 footprint for ME request
EC-B-17	9,18,22 23,33	11/10/14	Q30,Q31,Q26,Q27,Q34,Q35,Q3,Q4, Q41,Q42,Q23,Q24 DEL Add Q52,Q53,Q54,Q55,Q56,Q57 and ASM	Change MOS to Dual MOS
EC-B-18	21	11/10/19	Add Q58	For PS8622 flash ROM by EC ROM
EC-B-19	05	11/10/19	Add C727	Add a 10UF CAP for INTEL suggestion
EC-B-20	21	11/10/19	L14,L15,L16	Change footprint to 0603
EC-B-21	27	11/10/20	CN3	Change footprint for ME request
EC-B-22	36	11/10/24	Add C729,C730,C731	For EMI request
EC-B-23	3,7,11	11/10/24		Change LVDS singal by PCH provide
EC-B-24	7,24,25 26,27,29 30,31,33	11/10/24	R602,R322,R274,R305,R582,R580, L10,R129,R88,R87,R99,R79,R78, L22,L24	Change to short PAD
EC-B-25	8	11/10/24	BT1	Change BT1 footprint
EC-B-26	25	11/10/24	CN8	CN8 PIN4,5,7,8 connect to GND
EC-B-27	11,15	11/10/24	CML1,CML2,CML4,CML5 ASM R505,R502,R560,R563,R232,R233 R234,R235,C486,C488,C490,C497	for EMI request
EC-B-28	35	11/10/25	C472, C471, C470,C469,C681, C682 C683, C684,C685 ASM 0.1U	for EMI request
EC-B-29	35	11/10/25	RV5,C402 ASM 30P R194,R197 change to Bead	for EMI request
EC-B-30	35	11/10/26	C460 ASM 22P	for EMI request

A